

SEPS525

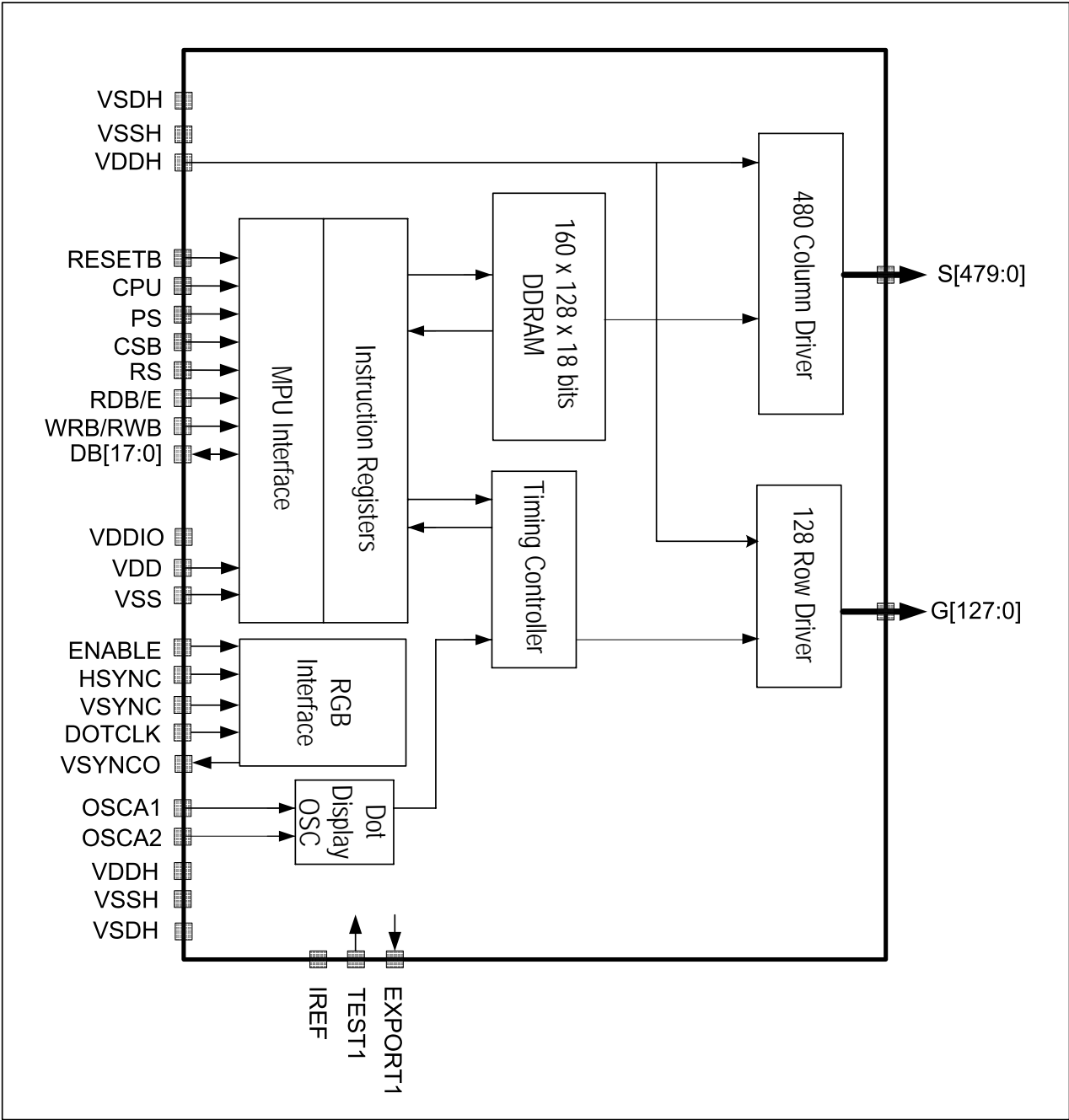
160 RGB x 128 Dots, 262K Colors PM-OLED Display Driver and Controller

1. Product Preview

- 262k colors OLED single chip display driver IC
- Data Interface
 - Parallel interface : 68/80series MPU(8/9/16/18-bit)
 - Serial interface : SPI 4-wire interface
 - RGB interface : 18/16/6-bit interface
- Driver Output
 - 160× RGB columns(480), 128 rows
- Display RAM Capacity
 - $160 \times 18(\text{RGB}) \times 128 = 368,640$ bits
- Various Instructions Set
 - Power save mode
 - Reduced current driving available
 - Window mode
 - Partial display : programmable panel display size
 - Vertical scroll & Horizontal panning
- OLED Column Drive
 - Driving current control : 8-bit, 0uA ~ 255uA by 1uA step control
 - Pre_charge current control : 8-bit, 0uA ~ 2040uA by 8uA step control
 - Pre_charge time control : programmable pre_charge time(0clock ~ 15clocks) based on internal oscillator clock
- OLED Row Drive
 - Current sink : Max 120mA
- Internal Oscillator Circuit
 - Internal / External clock selectable
 - Frame rate : 90 frames/sec(75.0 ~ 150.0 frames/sec adjustable)
- Supply Voltage
 - VDD : 2.4 ~ 3.3V
 - VDDH : 8.0 ~ 18.0V
 - VDDIO : 1.6 ~ 3.3V
- Package : Au Bumped
- Ordering information

| | |
|------------|-------------|
| SEPS525F0A | COF Package |
|------------|-------------|

2. Block Diagram



Block Diagram

3. Pin Description

| Pin Name | Number Of Pins | I/O | Connected To | Description | | | | | | |
|----------|---|-----|----------------------|---|----|-------------|---|---|---|---|
| CPU | 1 | I | VSS or VDD | Selects the CPU type Low : 80-Series CPU, High : 68-Series CPU | | | | | | |
| PS | 1 | I | VSS or VDD | Selects parallel/Serial interface type Low : serial, High : parallel | | | | | | |
| CSB | 1 | I | MPU | Selects the SEPS525. Low : SEPS525 is selected and can be accessed High : SEPS525 is not selected and cannot be accessed | | | | | | |
| RS | 1 | I | MPU | Selects the data / command Low : command, High : parameter / data | | | | | | |
| RDB/E | 1 | I | MPU | For an 80-system bus interface, read strobe signal(active low) For an 68-system bus interface, bus enable strobe(active high) When using SPI, fix it to VDD or VSS level | | | | | | |
| WRB/RWB | 1 | I | MPU | For an 80-system bus interface, write strobe signal(active low) For an 68-system bus interface, read/write select Low : Write, High : Read When using SPI, fix it to VDD or VSS level | | | | | | |
| DB[17:0] | 18 | I/O | MPU | Serves as a 18_bit bi-directional data bus <table border="1"><thead><tr><th>PS</th><th>Description</th></tr></thead><tbody><tr><td>1</td><td>8_bit bus : DB[17:10] 9_bit bus : DB[17:9] 16_bit bus : DB[17:10], DB[8:1] 18_bit bus : DB[17:0]</td></tr><tr><td>0</td><td>DB[17] SCL : Synchronous clock input DB[16] SDI : Serial data input DB[15] SDO : Serial data output</td></tr></tbody></table> Fix unused pins to the VSS level | PS | Description | 1 | 8_bit bus : DB[17:10] 9_bit bus : DB[17:9] 16_bit bus : DB[17:10], DB[8:1] 18_bit bus : DB[17:0] | 0 | DB[17] SCL : Synchronous clock input DB[16] SDI : Serial data input DB[15] SDO : Serial data output |
| PS | Description | | | | | | | | | |
| 1 | 8_bit bus : DB[17:10] 9_bit bus : DB[17:9] 16_bit bus : DB[17:10], DB[8:1] 18_bit bus : DB[17:0] | | | | | | | | | |
| 0 | DB[17] SCL : Synchronous clock input DB[16] SDI : Serial data input DB[15] SDO : Serial data output | | | | | | | | | |
| OSCA1 | 1 | I | Oscillation-Resistor | Fine adjustment for oscillation | | | | | | |
| OSCA2 | 1 | O | | Tie TBD kΩ ohms to OSCA1 between OSCA2 When the external clock mode is selected, OSCA1 is used external clock input | | | | | | |
| RESETB | 1 | I | MPU | Reset SEPS525(active low) | | | | | | |
| S[479:0] | 480 | O | PANEL | SEPS525 Display column outputs | | | | | | |
| G[127:0] | 128 | O | PANEL | SEPS525 Display row outputs | | | | | | |
| VDDH | 2 | - | POWER | Data, Scan Driver Power Supply(8V ~ 18V) | | | | | | |
| VSSH | 2 | - | POWER | Scan Driver Ground | | | | | | |
| VSDH | 2 | - | POWER | Data Driver Ground | | | | | | |
| VDDIO | 1 | - | POVER | MPU I/F PAD Power Supply(1.6 ~ 3.3V) | | | | | | |
| VDD | 1 | - | POWER | Logic power supply(2.4V ~ 3.3V) | | | | | | |
| VSS | 1 | - | POWER | Logic ground. | | | | | | |
| IREF | 1 | - | Resistor | Tie 70 kΩ to VSS | | | | | | |
| TEST1 | 1 | I | VSS or VDD | Selects the test mode | | | | | | |
| EXPORT1 | 1 | O | - | OSC Test | | | | | | |
| VSYNCO | 1 | O | - | Vertical Sync. Output | | | | | | |
| VSYNC | 1 | I | - | Vertical Sync. Input when RGB mode is selected | | | | | | |
| HSYNC | 1 | I | - | Horizontal Sync. Input when RGB mode is selected | | | | | | |
| DOTCLK | 1 | I | - | Dot clock Input when RGB mode is selected | | | | | | |
| ENABLE | 1 | I | - | Video enable Input when RGB mode is selected | | | | | | |

4. Functional Description

MPU Interface

The SEPS525 has three high-speed system interface : a 68-system, an 80-system 8/9/16/18 bit bus, and a clock synchronous serial(SPI : Serial Peripheral Interface). Among the interface modes, a specific mode is selected by the setting of PS pin and MEMORY_WRITE_MODE register(16h).

The SEPS525 has 3-type registers : an index register(IR) 8-bits, a write data register(WDR), and a read data register(RDR). The IR stores index information for the control registers and the DDRAM. The WDR temporarily stores data to be written into control registers and the DDRAM, and the RDR temporarily stores data read from the DDRAM.

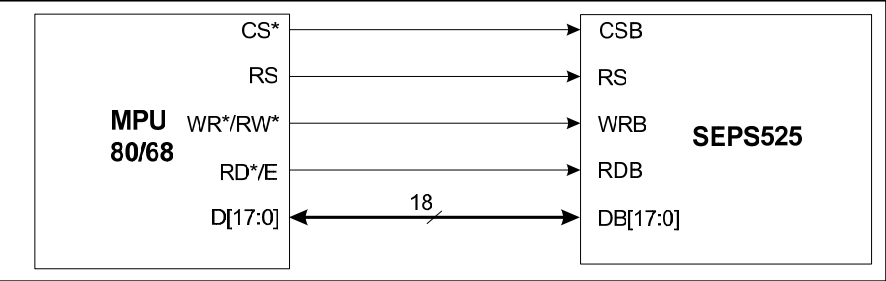
Data written into the DDRAM from the MPU is first written into the WDR and then it is automatically written into the DDRAM by internal operation. Data is read through the RDR when reading from the DDRAM, and the first read data is invalid and the second and the following data are valid.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

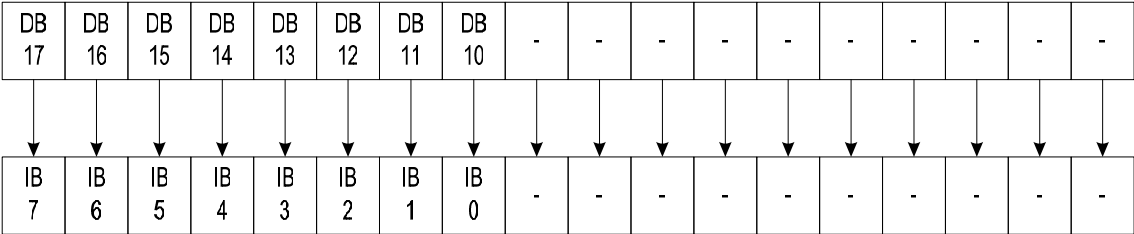
| RS | 80 mode | | 68 mode | | Operation |
|----|---------|-----|---------|---|---|
| | RDB | WRB | RWB | E | |
| 0 | 0 | 1 | 1 | 1 | Reads internal status |
| 0 | 1 | 0 | 0 | 1 | Writes indexes into IR |
| 1 | 0 | 1 | 1 | 1 | Reads from DDRAM through RDR |
| 1 | 1 | 0 | 0 | 1 | Writes into control registers and DDRAM through WDR |

1) 18-bit Bus Interface(Index 16h)

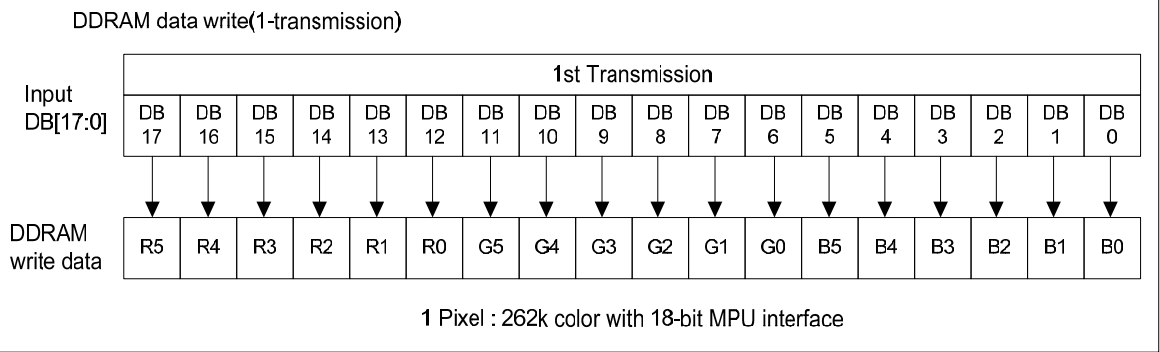
| DFM1 | DFM0 | TRI | Operation |
|------|------|-----|----------------------|
| 0 | 0 | x | 18-bit bus operation |



Index/Command Write

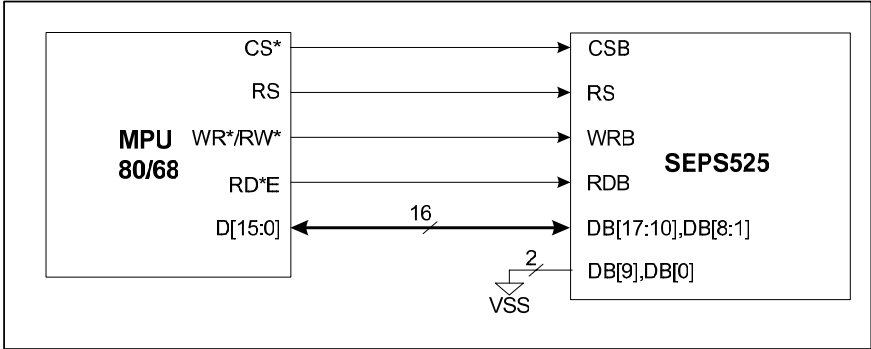


DDRAM Read/Write

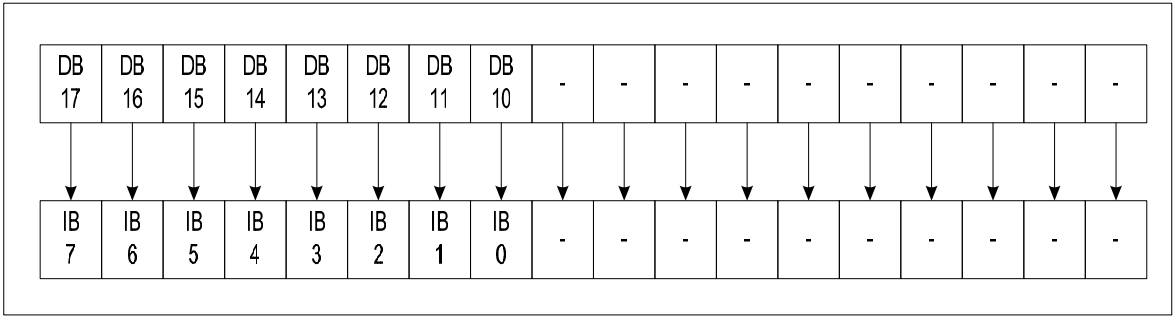


2) 16-bit Bus Interface

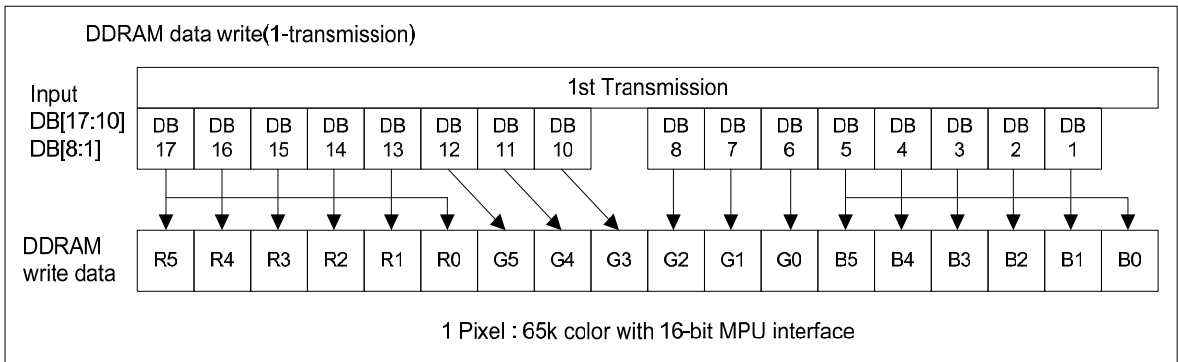
| DFM1 | DFM0 | TRI | Operation |
|------|------|-----|----------------------|
| 0 | 1 | x | 16-bit bus operation |



Index/Command Write

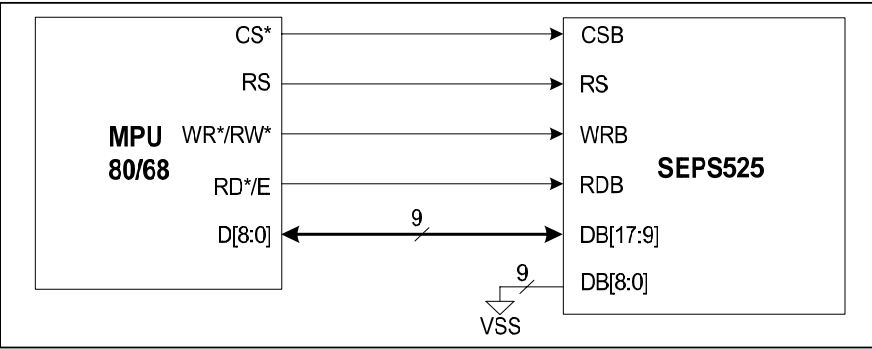


DDRAM Read/Write

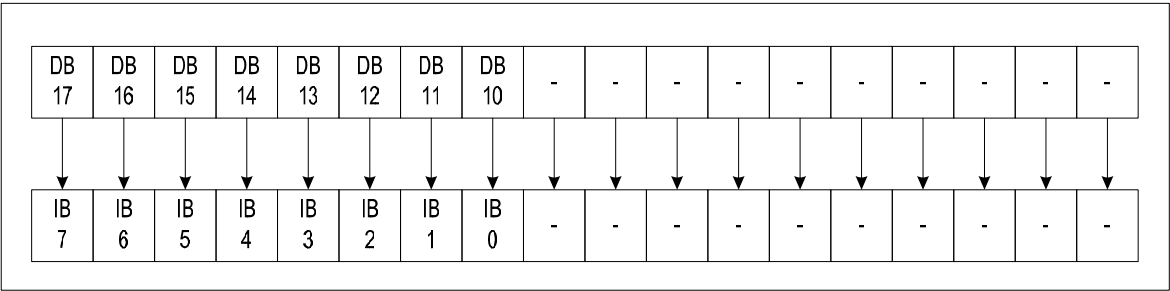


3) 9-bit Bus Interface

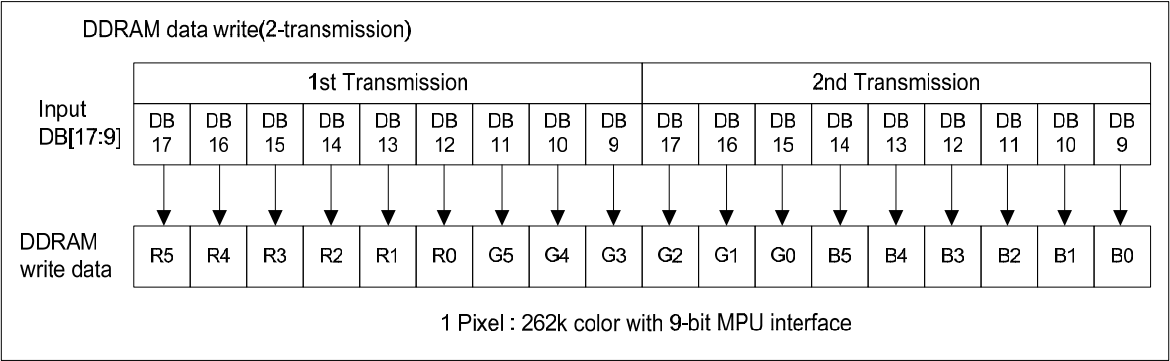
| DFM1 | DFM0 | TRI | Operation |
|------|------|-----|---------------------|
| 1 | 0 | x | 9-bit bus operation |



Index/Command Write

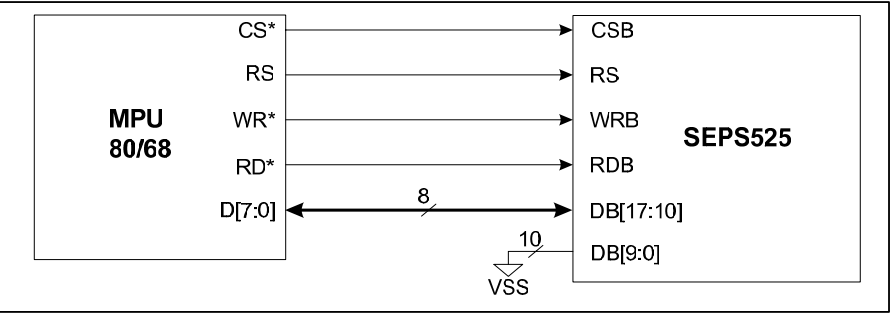


DDRAM Read/Write

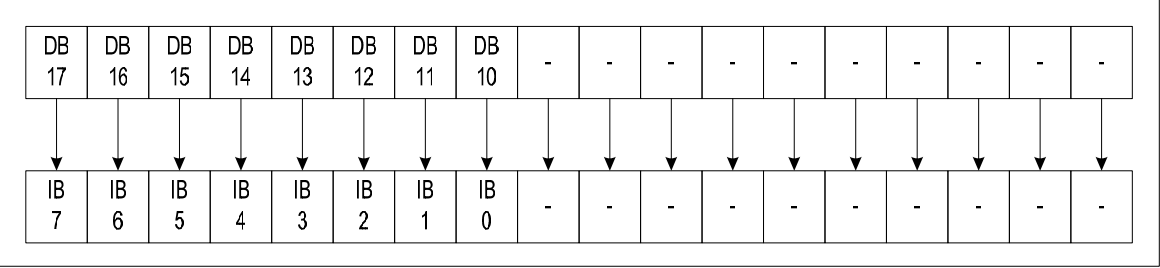


4) 8-bit Bus Interface

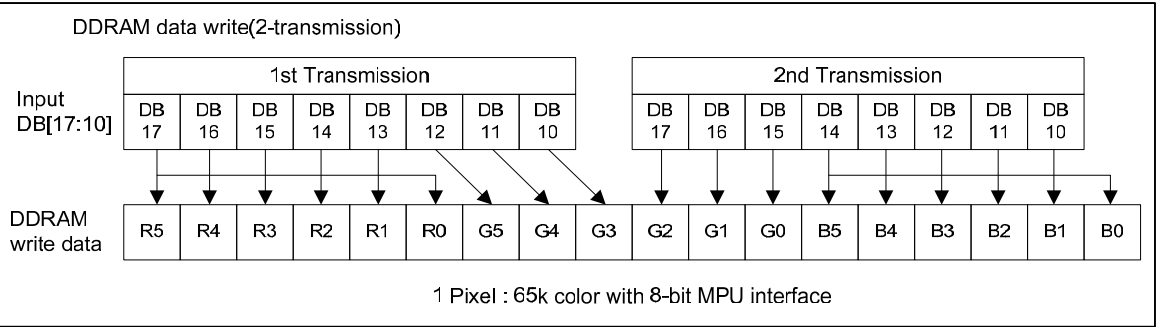
| DFM1 | DFM0 | TRI | Operation |
|------|------|-----|--------------|
| 1 | 0 | 0 | Dual 8-bit |
| 1 | 1 | 1 | Triple 6-bit |



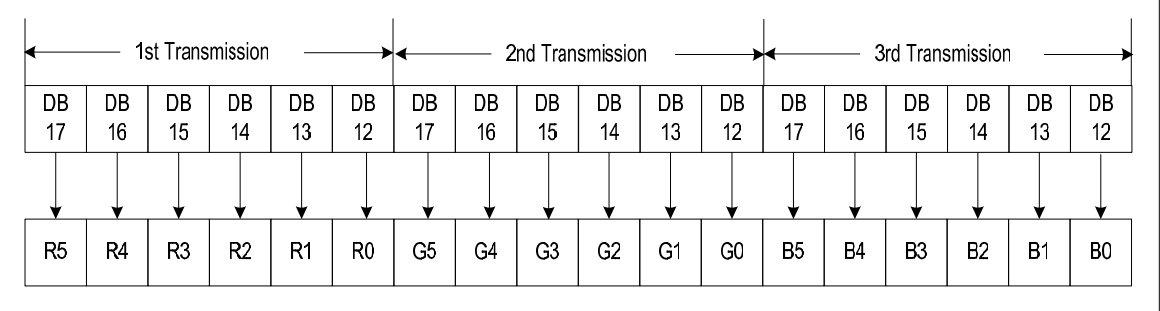
Index/Command Write



DDRAM Write/Read



DDRAM Write/Read (TRI mode)



5) Clock Synchronized Serial Interface (SPI)

Setting PS pin to the "0" level allows clock synchronized serial data(SPI) transfer, using the chip select pin(CSB), RS pin, serial transfer clock pin(SCL) and serial data input(SDI).

When chip is not selected, internal shift register and counter is resets to initial value. Input data through SDI pin are latched at the rising edge of serial transfer clock(SCL). SDI inputs are converted to 16-bit or 18-bit data and transferred to memory at the 16th/18th rising edge serial clock, respectively.

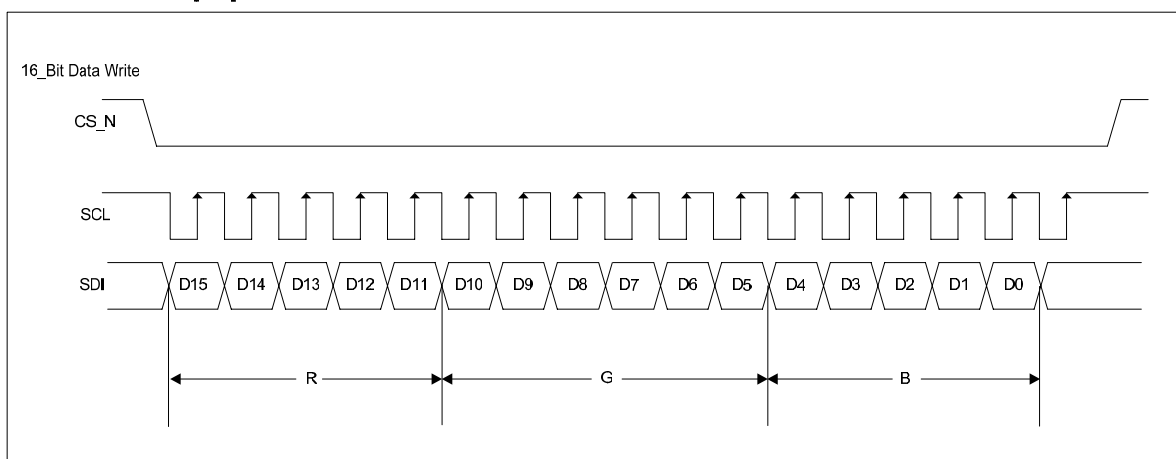
Serial data input(SDI) is identified to display data or command by RS pin.

| RS | Function |
|----|-----------------|
| L | Command |
| H | Parameter/ Data |

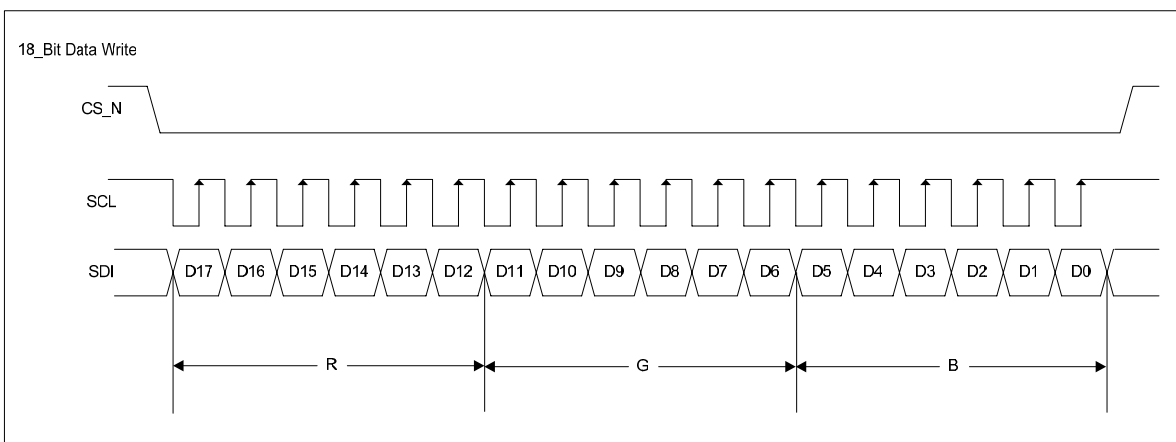
after 8-bit data transfer, serial transfer clock(SCL) goes to "H" at the non-access period. SDI and SCL signals are sensitive to external noise. To prevent miss operation chip selector state should be released(CSB = "H") after 8-bit data transfer as shown in the following.

*Note : When the SPI mode is selected, DB[15] pin must be unconnected.

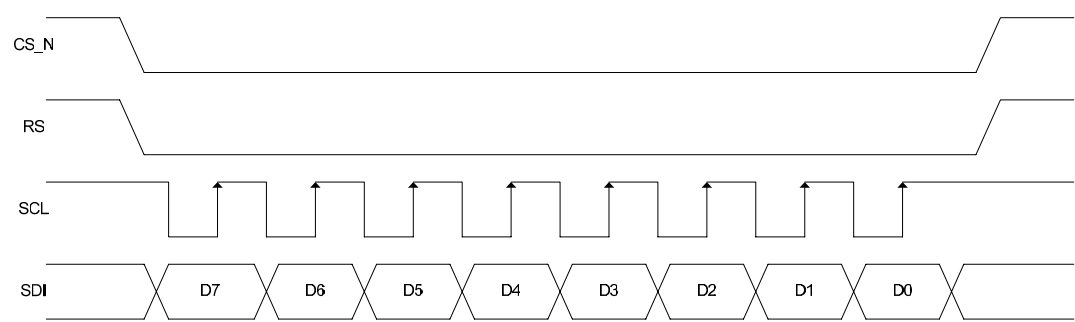
PS = "0", DFM[1:0] = "11", TRI = "0"



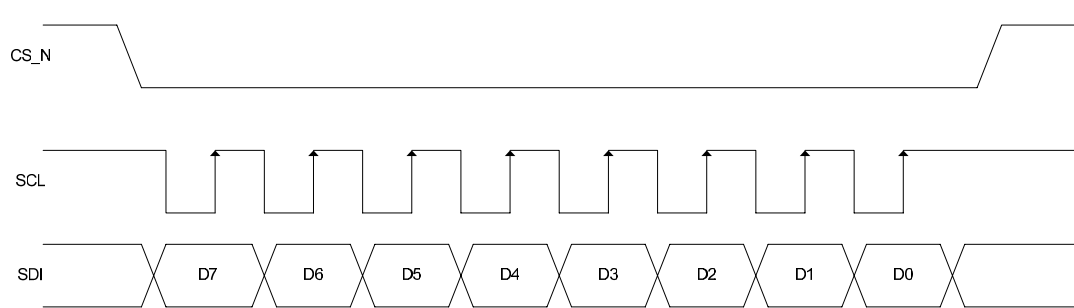
PS = "0", DFM[1:0] = "11", TRI = "1"



INDEX REGISTER WRITE

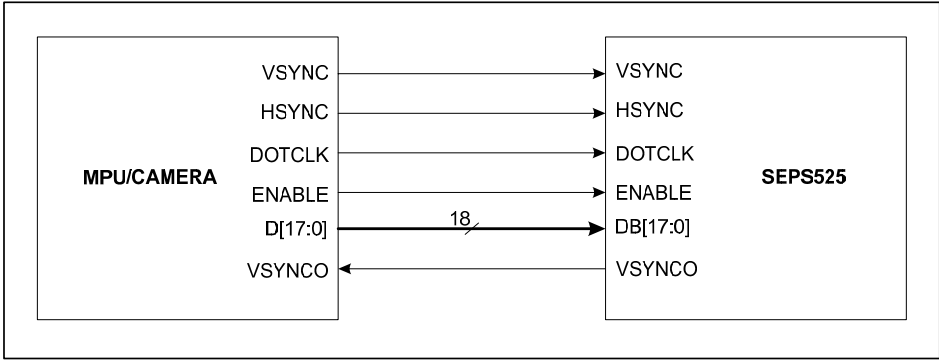


CONTROL REGISTER WRITE



6) RGB Interface

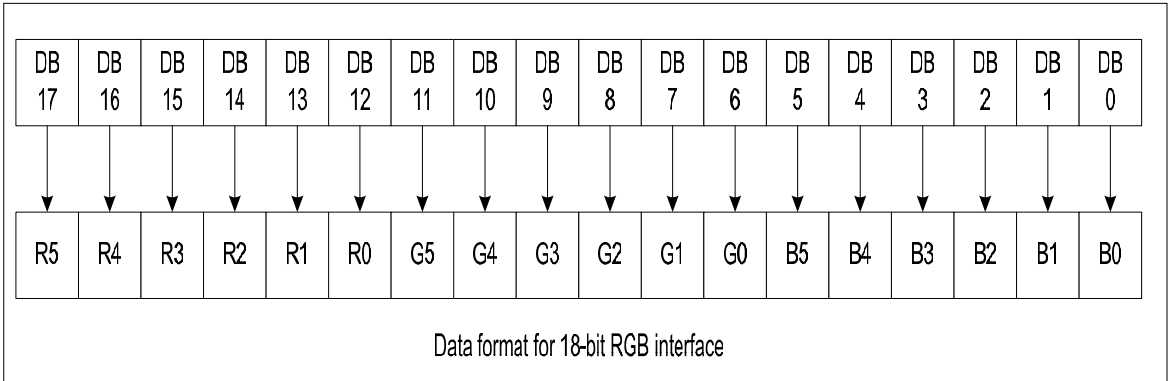
When the RGB_IF register bit0 is set to “0”, SEPS525 enters into the RGB interface mode and DDRAM write cycle is synchronized by DOTCLK.



18-bit RGB interface

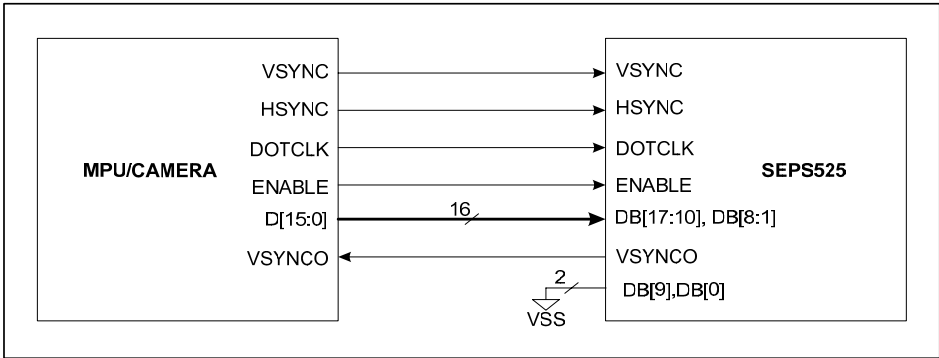
The 18-bit RGB interface is selected by setting RIM[1:0] bits to “00”. DDRAM write operation is Synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 18-bit RGB data bus(DB[17:0]) and the data enable(ENABLE).

DDRAM Write

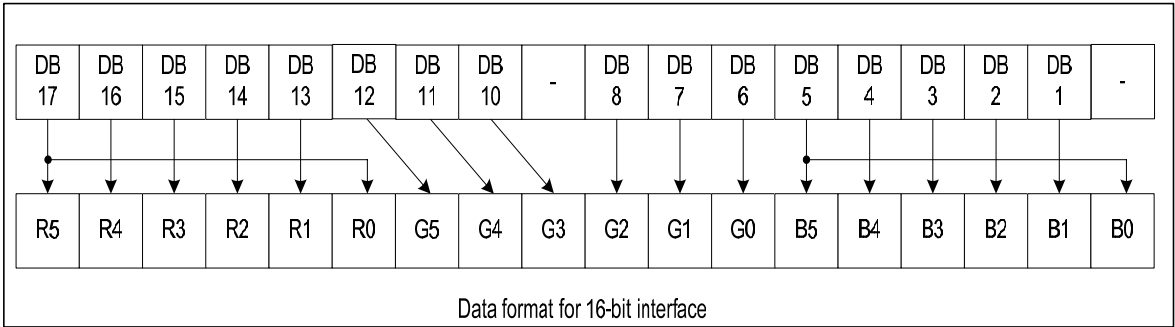


16-bit RGB interface

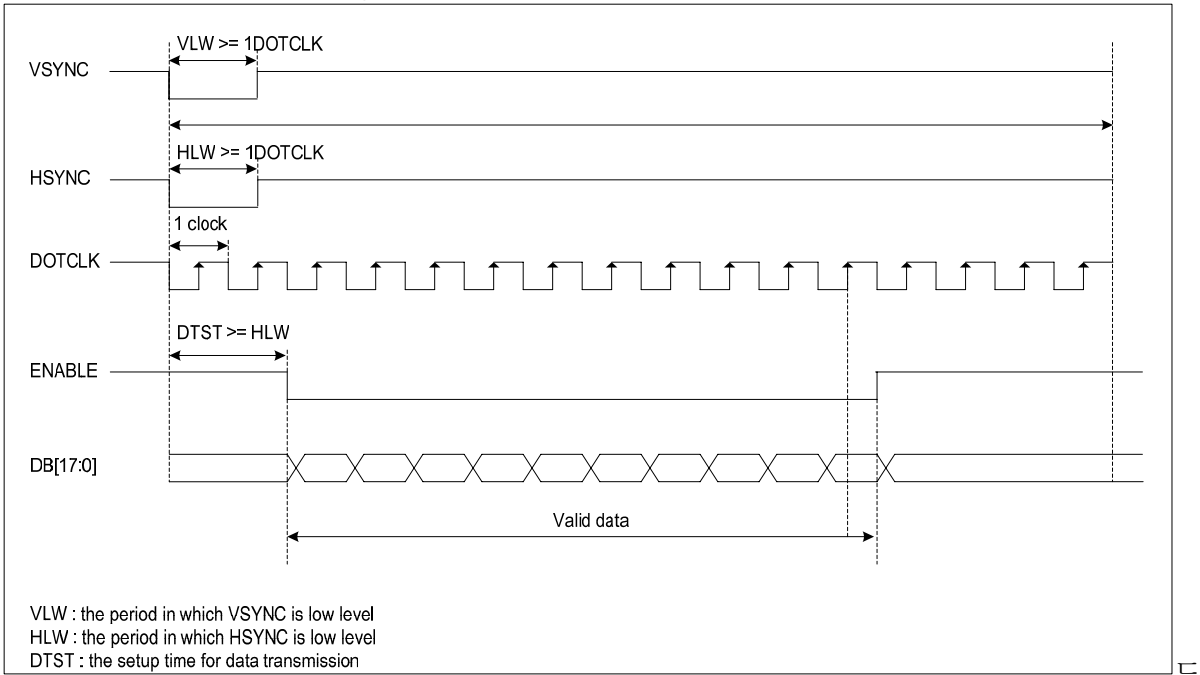
The 16-bit RGB interface is selected by setting RIM[1:0] bits to “01”. DDRAM write operation is Synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 16-bit RGB data bus(DB[17:10], DB[8:1]) and the data enable(ENABLE).



DDRAM Write

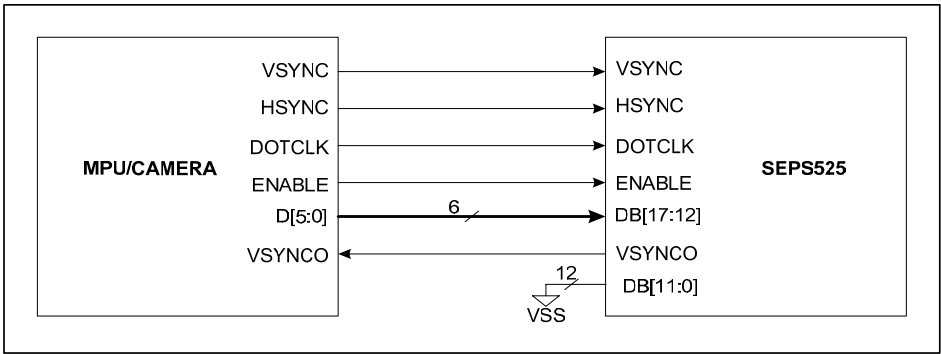


18/16-bit RGB interface timing

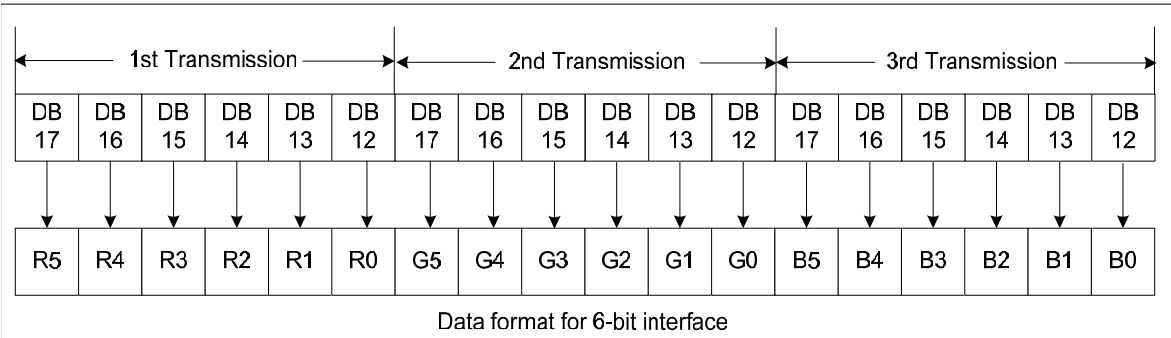


6-bit RGB interface

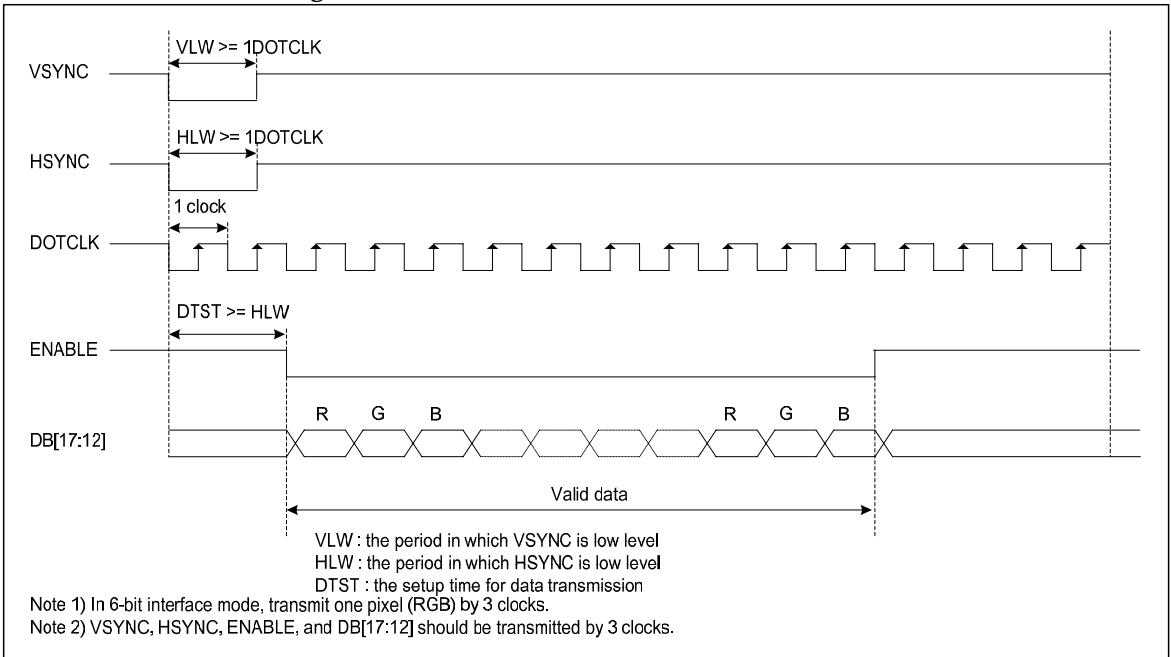
The 6-bit RGB interface is selected by setting RIM[1:0] bits to “10”. DDRAM write operation is Synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 6-bit RGB data bus(DB[17:12]) and the data enable(ENABLE).



DDRAM Write



6-bit RGB interface timing

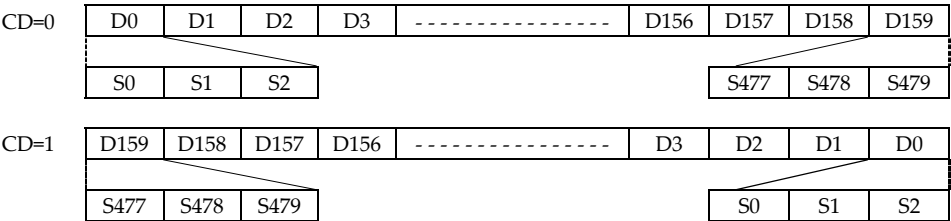


DDRAM(Display Data RAM) Addressing

The DDRAM stores pixel data for the display. It is composed of 128-row by 160-column x 18-bit addressable array. Address counter provides row and column address to DDRAM for access display pixel data from MPU.

Relationship Between DDRAM Address and Display Position

| | | | | | | | | | | | |
|------|------|-------------|---|---|---|---|-------|-----|-----|-----|-----|
| G0 | G127 | 00h | | | | | ----- | | | | |
| G1 | G126 | 01h | | | | | | | | | |
| G2 | G125 | 02h | | | | | | | | | |
| G3 | G124 | 03h | | | | | | | | | |
| G4 | G123 | 04h | | | | | | | | | |
| G5 | G122 | 05h | | | | | | | | | |
| . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . |
| G122 | G5 | 79h | | | | | | | | | |
| G123 | G4 | 7Ah | | | | | | | | | |
| G124 | G3 | 7Bh | | | | | | | | | |
| G125 | G2 | 7Ch | | | | | | | | | |
| G126 | G1 | 7Eh | | | | | | | | | |
| G127 | G0 | 7Fh | | | | | | | | | |
| RD=0 | RD=1 | Column Data | 0 | 1 | 2 | 3 | ----- | 156 | 157 | 158 | 159 |



RD : Row scan shift direction register bit.
CD : Column data shift direction register bit.

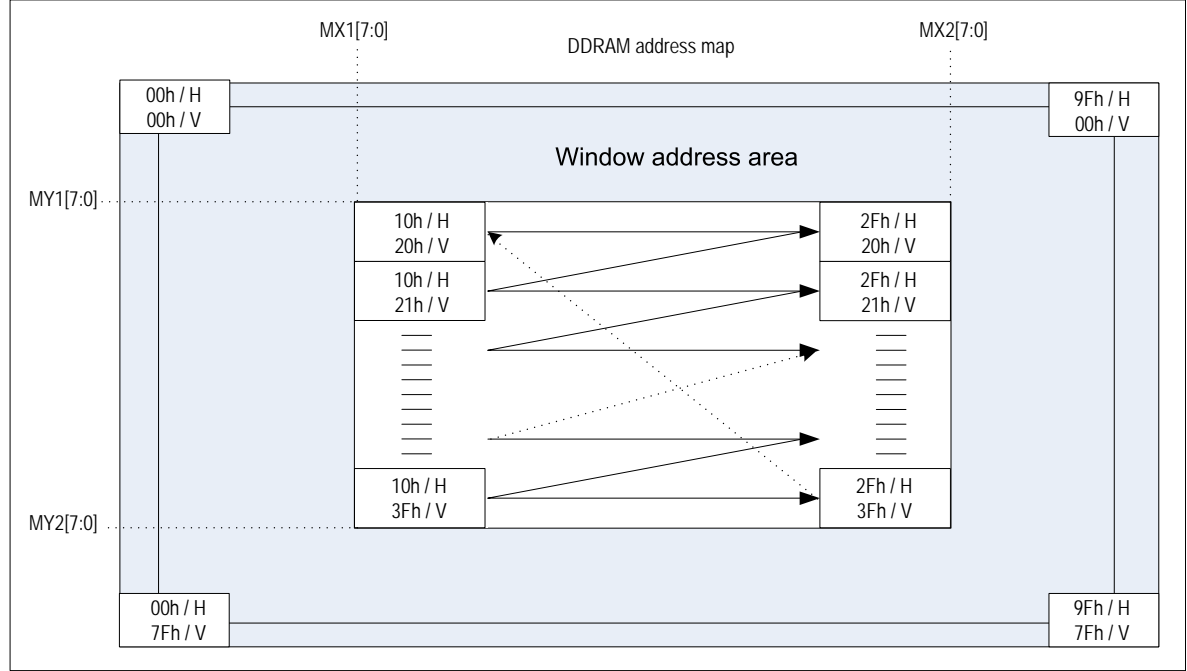
Window Address Function

When data is written to the on-chip DDRAM, a window address-range which is specified by the horizontal address register(start : MX1[7:0], end : MX2[7:0]) or the vertical address register(start : MY1[7:0], end : MY2[7:0]) can be written to consecutively. Data is written to addresses in the direction specified by the HC, VC(increment/decrement), and HV bit(H or V direction). When the image data is being written, data can be written consecutively without thinking of a data wrap by doing this.
The window must be specified within the DDRAM address area described below, Addresses must be set within the window address.

[Restriction on window address-range setting]
(horizontal direction) $00h \leq MX1[7:0] < MX2[7:0] \leq 9Fh$
(vertical direction) $00h \leq MY1[7:0] < MY2[7:0] \leq 7Fh$

Window address-range specification.
MX1[7:0] = 10h, MY1[7:0] = 2Fh
MY1[7:0] = 20h, MY2[7:0] = 3Fh
HC, VC = 1,1 (increment)
HV = 0 (horizontal writing)

Example of Address Operation in the Window Address Specification



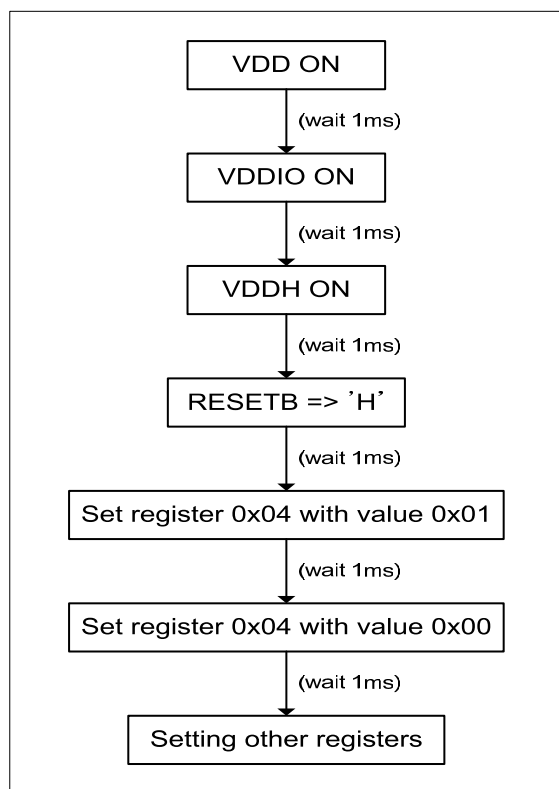
Reset Status

The **SEPS525** is initialized as following description when RESETB terminal is set to “L”. Usually RESETB terminal is connected reset terminal of MPU, so that the chip can be initialized simultaneously with MPU. The **SEPS525** should be initialized when the power is on.

INITIAL SETTING CONDITION (default setting)

1. Frame frequency : 90Hz
2. OSC : internal OSC
3. Internal OSC : ON
4. DDRAM write horizontal address : MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address : MY1 = 00h, MY2 = 7Fh
6. Display data RAM write : HC = 1, VC = 1, HV = 0
7. RGB data swap : OFF
8. Row scan shift direction : G0, G1, ... , G126, G127
9. Column data shift direction : S0, S1, ... , S478, S479
10. Display ON/OFF : OFF
11. Panel display size : FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address : FAC = 00h, FAR = 00h
13. Precharge time(R/G/B) : 0 clock
14. Precharge current(R/G/B) : 0 uA
15. Driving current(R/G/B) : 0 uA

POWER ON SEQUENCE



5. Instruction Description

Normal Display

| ADDR | RW | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | Description | Default |
|------|-----|-------------|---------|---------|---------|---------|---------|---------|---------|--------------------------|---------|
| 00h | R | IDX7 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | INDEX | 00h |
| 01h | R | HC | VC | HV | SWAP | RD | CD | DC1 | DC0 | STATUS_RD | C0h |
| 02h | R/W | SELEXP | SELRES | 0 | 0 | 0 | 0 | SELCLK | OSCDSB | OSC_CTL | C0h |
| 03h | R/W | FR3 | FR2 | FR1 | FR0 | DFR3 | DFR2 | DFR1 | DFR0 | CLOCK_DIV | 30h |
| 04h | R/W | 0 | 0 | 0 | 0 | 0 | RC | OSCP5 | PS | REDUCE_CURRENT | 00h |
| 05h | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SRN | SOFT_RST | 00h |
| 06h | R/W | PREM | 0 | 0 | 0 | 0 | 0 | 0 | DON | DISP_ON_OFF | 00h |
| 08h | R/W | 0 | 0 | 0 | 0 | PTR3 | PTR2 | PTR1 | PTR0 | PRECHARGE_TIME_R | 00h |
| 09h | R/W | 0 | 0 | 0 | 0 | PTG3 | PTG2 | PTG1 | PTG0 | PRECHARGE_TIME_G | 00h |
| 0Ah | R/W | 0 | 0 | 0 | 0 | PTB3 | PTB2 | PTB1 | PTB0 | PRECHARGE_TIME_B | 00h |
| 0Bh | R/W | PCR7 | PCR6 | PCR5 | PCR4 | PCR3 | PCR2 | PCR1 | PCR0 | PRECHARGE_CURRENT_R | 00h |
| 0Ch | R/W | PCG7 | PCG6 | PCG5 | PCG4 | PCG3 | PCG2 | PCG1 | PCG0 | PRECHARGE_CURRENT_G | 00h |
| 0Dh | R/W | PCB7 | PCB6 | PCB5 | PCB4 | PCB3 | PCB2 | PCB1 | PCB0 | PRECHARGE_CURRENT_B | 00h |
| 10h | R/W | DCR7 | DCR6 | DCR5 | DCR4 | DCR3 | DCR2 | DCR1 | DCR0 | DRIVING_CURRENT_R | 00h |
| 11h | R/W | DCG7 | DCG6 | DCG5 | DCG4 | DCG3 | DCG2 | DCG1 | DCG0 | DRIVING_CURRENT_G | 00h |
| 12h | R/W | DCB7 | DCB6 | DCB5 | DCB4 | DCB3 | DCB2 | DCB1 | DCB0 | DRIVING_CURRENT_B | 00h |
| 13h | R/W | SWAP | SM | RD | CD | 0 | SPT | DC1 | DC0 | DISPLAY_MODE_SET | 00h |
| 14h | R/W | 0 | 0 | RIM1 | RIM0 | 0 | 0 | 0 | EIM | RGB_IF | 11h |
| 15h | R/W | RES | RES | ENP | DOP | VSYOEN | RES | RES | RES | RGB_POL | 00h |
| 16h | R/W | 0 | DFM1 | DFM0 | TRI | 0 | HC | VC | HV | MEMORY_WRITE_MODE | 06h |
| 17h | R/W | MX1_7 | MX1_6 | MX1_5 | MX1_4 | MX1_3 | MX1_2 | MX1_1 | MX1_0 | MX1_ADDR | 00h |
| 18h | R/W | MX2_7 | MX2_6 | MX2_5 | MX2_4 | MX2_3 | MX2_2 | MX2_1 | MX2_0 | MX2_ADDR | 9Fh |
| 19h | R/W | MY1_7 | MY1_6 | MY1_5 | MY1_4 | MY1_3 | MY1_2 | MY1_1 | MY1_0 | MY1_ADDR | 00h |
| 1Ah | R/W | MY2_7 | MY2_6 | MY2_5 | MY2_4 | MY2_3 | MY2_2 | MY2_1 | MY2_0 | MY2_ADDR | 7Fh |
| 20h | R/W | MAC7 | MAC6 | MAC5 | MAC4 | MAC3 | MAC2 | MAC1 | MAC0 | MEMORY_ACCESS_POINTER X | 00h |
| 21h | R/W | MAR7 | MAR6 | MAR5 | MAR4 | MAR3 | MAR2 | MAR1 | MAR0 | MEMORY_ACCESS_POINTER Y | 00h |
| 22h | | DDRAM[17:0] | | | | | | | | DDRAM_DATA_ACCESS_PORT | |
| 50h | R/W | IGAMMA7 | IGAMMA6 | IGAMMA5 | IGAMMA4 | IGAMMA3 | IGAMMA2 | IGAMMA1 | IGAMMA0 | GRAY_SCALE_I_TABLE_INDEX | 00h |
| 51h | R/W | DGAMMA7 | DGAMMA6 | DGAMMA5 | DGAMMA4 | DGAMMA3 | DGAMMA2 | DGAMMA1 | DGAMMA0 | GRAY_SCALE_I_TABLE_DATA | |
| 28h | R/W | DUTY7 | DUTY6 | DUTY5 | DUTY4 | DUTY3 | DUTY2 | DUTY1 | DUTY0 | DUTY | 7Fh |
| 29h | R/W | DSL7 | DSL6 | DSL5 | DSL4 | DSL3 | DSL2 | DSL1 | DSL0 | DSL | 00h |
| 2Eh | R/W | FAC7 | FAC6 | FAC5 | FAC4 | FAC3 | FAC2 | FAC1 | FAC0 | D1_DDRAM_FAC | 00h |
| 2Fh | R/W | FAR7 | FAR6 | FAR5 | FAR4 | FAR3 | FAR2 | FAR1 | FAR0 | D1_DDRAM_FAR | 00h |
| 31h | R/W | SAC7 | SAC6 | SAC5 | SAC4 | SAC3 | SAC2 | SAC1 | SAC0 | D2_DDRAM_SAC | 00h |
| 32h | R/W | SAR7 | SAR6 | SAR5 | SAR4 | SAR3 | SAR2 | SAR1 | SAR0 | D2_DDRAM_SAR | 00h |
| 33h | R/W | FX1_7 | FX1_6 | FX1_5 | FX1_4 | FX1_3 | FX1_2 | FX1_1 | FX1_0 | SCR1_FX1 | 00h |
| 34h | R/W | FX2_7 | FX2_6 | FX2_5 | FX2_4 | FX2_3 | FX2_2 | FX2_1 | FX2_0 | SCR1_FX2 | 9Fh |
| 35h | R/W | FY1_7 | FY1_6 | FY1_5 | FY1_4 | FY1_3 | FY1_2 | FY1_1 | FY1_0 | SCR1_FY1 | 00h |
| 36h | R/W | FY2_7 | FY2_6 | FY2_5 | FY2_4 | FY2_3 | FY2_2 | FY2_1 | FY2_0 | SCR1_FY2 | 7Fh |
| 37h | R/W | SX1_7 | SX1_6 | SX1_5 | SX1_4 | SX1_3 | SX1_2 | SX1_1 | SX1_0 | SCR2_SX1 | 00h |
| 38h | R/W | SX2_7 | SX2_6 | SX2_5 | SX2_4 | SX2_3 | SX2_2 | SX2_1 | SX2_0 | SCR2_SX2 | 9Fh |
| 39h | R/W | SY1_7 | SY1_6 | SY1_5 | SY1_4 | SY1_3 | SY1_2 | SY1_1 | SY1_0 | SCR2_SY1 | 00h |
| 3Ah | R/W | SY2_7 | SY2_6 | SY2_5 | SY2_4 | SY2_3 | SY2_2 | SY2_1 | SY2_0 | SCR2_SY2 | 7Fh |
| 3Bh | R/W | 0 | SSA1 | SSA0 | 0 | SSC1 | SSC0 | 0 | SSM | SCREEN_SAVER_CONTEROL | 00h |
| 3Ch | R/W | SST7 | SST6 | SST5 | SST4 | SST3 | SST2 | SST1 | SST0 | SS_SLEEP_TIMER | 00h |
| 3Dh | R/W | 0 | 0 | SMS1 | SMS0 | 0 | 0 | SMF1 | SMF0 | SCREEN_SAVER_MODE | 00h |
| 3Eh | R/W | FSUT7 | FSUT6 | FSUT5 | FSUT4 | FSUT3 | FSUT2 | FSUT1 | FSUT | SS_SCR1_FU | 00h |
| 3Fh | R/W | FSMS7 | FSMS6 | FSMS5 | FSMS4 | FSMS3 | FSMS2 | FSMS1 | FSMS0 | SS_SCR1_MXY | 00h |
| 40h | R/W | SSUT7 | SSUT6 | SSUT5 | SSUT4 | SSUT3 | SSUT2 | SSUT1 | SSUT0 | SS_SCR2_FU | 00h |
| 41h | R/W | SSMS7 | SSMS6 | SSMS5 | SSMS4 | SSMS3 | SSMS2 | SSMS1 | SSMS0 | SS_SCR2_MXY | 00h |
| 42h | R/W | 0 | 0 | SSMD1 | SSMD0 | 0 | 0 | FSMD1 | FSMD0 | MOVING_DIRECTION | 00h |
| 47h | R/W | ISX1_7 | ISX1_6 | ISX1_5 | ISX14 | ISX1_3 | ISX1_2 | ISX1_1 | ISX1_0 | SS_SCR2_SX1 | 00h |
| 48h | R/W | ISX2_7 | ISX2_6 | ISX2_5 | ISX2_4 | ISX2_3 | ISX2_2 | ISX2_1 | ISX2_0 | SS_SCR2_SX2 | 00h |
| 49h | R/W | ISY1_7 | ISY1_6 | ISY1_5 | ISY1_4 | ISY1_3 | ISY1_2 | ISY1_1 | ISY1_0 | SS_SCR2_SY1 | 00h |
| 4Ah | R/W | ISY2_7 | ISY2_6 | ISY2_5 | ISY2_4 | ISY2_3 | ISY2_2 | ISY2_1 | ISY2_0 | SS_SCR2_SY2 | 00h |

INDEX (00h)

| R/W | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----|-------|------|------|------|------|------|------|------|
| R | IDX7 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 |

IDX[7:0] : Index address of registers.

STATUS_RD (01h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R | HC | VC | HV | SWAP | RD | CD | DC1 | DC0 |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The status read instruction reads the internal status of the SEPS525.

HC : Horizontal address increment/decrement at memory write mode.

VC : Vertical address increment/decrement at memory write mode.

HV : Automatic update method of the AC(means internal address counter).

HV=0(horizontal), HV=1(vertical)

SWAP : Swap between R and B.

RD : Row scan shift direction.

CD : Column data shift direction.

DC[1:0] : Display data output control.

OSC_CTL (02h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|--------|------|------|------|------|--------|--------|
| R/W | SELEXP | SELRES | - | - | - | - | SELCLK | OSCDSB |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

SELEXP : OSC

When SELEXP = 0, EXPORT1 internal clock

When SELEXP = 1, EXPORT1 "0" level

SELRES : Internal oscillator mode selection.

When SELRES = 0, Oscillator operates with external resister

When SELRES = 1, Oscillator operates with internal resister

SELCLK, OSCDSB :

| SELCLK | OSCDSB | |
|--------|--------|-------------------|
| X | 0 | CLOCK OFF |
| 0 | 1 | Internal OSC ON |
| 1 | 1 | External CLK mode |

IREF (80h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | - | - | - | - | - | IREF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IREF : Control reference voltage generation.

When IREF = 0, Reference voltage controlled by external resister

When IREF = 1, Reference voltage controlled by internal resister

CLOCK_DIV (03h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | FR3 | FR2 | FR1 | FR0 | DFR3 | DFR2 | DFR1 | DFR0 |
| Default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

FR[3:0] : OSC frequency setting.

| FR3 | FR2 | FR1 | FR0 | Frame Rate |
|----------|----------|----------|----------|--------------|
| 0 | 0 | 0 | 0 | 75 Hz |
| 0 | 0 | 0 | 1 | 80 Hz |
| 0 | 0 | 1 | 0 | 85 Hz |
| 0 | 0 | 1 | 1 | 90 Hz |
| 0 | 1 | 0 | 0 | 95 Hz |
| 0 | 1 | 0 | 1 | 100 Hz |
| 0 | 1 | 1 | 0 | 105 Hz |
| 0 | 1 | 1 | 1 | 110 Hz |

| FR3 | FR2 | FR1 | FR0 | Frame Rate |
|-----|-----|-----|-----|------------|
| 1 | 0 | 0 | 0 | 115 Hz |
| 1 | 0 | 0 | 1 | 120 Hz |
| 1 | 0 | 1 | 0 | 125 Hz |
| 1 | 0 | 1 | 1 | 130 Hz |
| 1 | 1 | 0 | 0 | 135 Hz |
| 1 | 1 | 0 | 1 | 140 Hz |
| 1 | 1 | 1 | 0 | 145 Hz |
| 1 | 1 | 1 | 1 | 150 Hz |

DFR[3:0] : Display frequency divide ration.

| DFR3 | DFR2 | DFR1 | DFR0 | OSC CLK |
|------|------|------|------|---------|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1/2 |
| 0 | 0 | 1 | 1 | 1/3 |
| 0 | 1 | 0 | 0 | 1/4 |
| 0 | 1 | 0 | 1 | 1/5 |
| 0 | 1 | 1 | 0 | 1/6 |
| 0 | 1 | 1 | 1 | 1/7 |

| DFR3 | DFR2 | DFR1 | DFR0 | OSC CLK |
|------|------|------|------|---------|
| 1 | 0 | 0 | 0 | 1/8 |
| 1 | 0 | 0 | 1 | 1/9 |
| 1 | 0 | 1 | 0 | 1/10 |
| 1 | 0 | 1 | 1 | 1/11 |
| 1 | 1 | 0 | 0 | 1/12 |
| 1 | 1 | 0 | 1 | 1/13 |
| 1 | 1 | 1 | 0 | 1/14 |
| 1 | 1 | 1 | 1 | 1/15 |

REDUCE_CURRENT (04h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|-------|------|
| R/W | - | - | - | - | - | RC | OSCPS | PS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RC : Reduced driving current.

When RC = 0, Normal

When RC = 1, 1/2driving current(address 0x10, 0x11, 0x12)

OSCPS : Oscillator power down

When OSCPS = 0, Normal

When OSCPS = 1, Internal oscillator power off

PS : Power save mode.

When PS = 0, normal

When PS = 1, display off, analog reset

SOFT_RST (05h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | - | - | - | - | - | SRN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SRN : Soft reset active high.

When SRN = 0, normal mode

When SRN = 1, all internal register value will be default

DISP_ON_OFF (06h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | PREM | - | - | - | - | - | - | DON |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PREM : Precharge mode select.

When PREM = 0, Scan signal is high level at pre_charge period

When PREM = 1, Scan signal is low level at pre_charge period

DON : Display ON/OFF.

When DON = 0, Turns the display off

When DON = 1, Turns the display on

PRECHARGE_TIME_R (08h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | - | - | PTR3 | PTR2 | PTR1 | PTR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PRECHARGE_TIME_G (09h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | - | - | PTG3 | PTG2 | PTG1 | PTG0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PRECHARGE_TIME_B (0Ah)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | - | - | PTB3 | PTB2 | PTB1 | PTB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PTR[3:0] : Precharge time R.

PTG[3:0] : Precharge time G.

PTB[3:0] : Precharge time B.

* PTR[3:0]/PTG[3:0]/PTB[3:0] is used for precharge time selection of Red/Green/Blue pixel.
The range is from 0 to 15 based on internal OSC.

| PTR3/ PRG3/ PRB3 | PTR2/ PRG2/ PRB2 | PTR1/ PRG1/ PRB1 | PTR0/ PRG0/ PRB0 | Precharge Time (CLK) |
|------------------------|------------------------|------------------------|------------------------|-------------------------|
| 0 | 0 | 0 | 0 | No Precharge Time (Clk) |
| 0 | 0 | 0 | 1 | 1 Precharge Time (Clk) |
| 0 | 0 | 1 | 0 | 2 Precharge Time (Clk) |
| 0 | 0 | 1 | 1 | 3 Precharge Time (Clk) |
| 0 | 1 | 0 | 0 | 4 Precharge Time (Clk) |
| 0 | 1 | 0 | 1 | 5 Precharge Time (Clk) |
| 0 | 1 | 1 | 0 | 6 Precharge Time (Clk) |
| 0 | 1 | 1 | 1 | 7 Precharge Time (Clk) |
| 1 | 0 | 0 | 0 | 8 Precharge Time (Clk) |
| 1 | 0 | 0 | 1 | 9 Precharge Time (Clk) |
| 1 | 0 | 1 | 0 | 10 Precharge Time (Clk) |
| 1 | 0 | 1 | 1 | 11 Precharge Time (Clk) |
| 1 | 1 | 0 | 0 | 12 Precharge Time (Clk) |
| 1 | 1 | 0 | 1 | 13 Precharge Time (Clk) |
| 1 | 1 | 1 | 0 | 14 Precharge Time (Clk) |
| 1 | 1 | 1 | 1 | 15 Precharge Time (Clk) |

PRECHARGE_CURRENT_R (0Bh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | PCR7 | PCR6 | PCR5 | PCR4 | PCR3 | PCR2 | PCR1 | PCR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PRECHARGE_CURRENT_G (0Ch)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | PCG7 | PCG6 | PCG5 | PCG4 | PCG3 | PCG2 | PCG1 | PCG0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PRECHARGE_CURRENT_B (0Dh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | PCB7 | PCB6 | PCB5 | PCB4 | PCB3 | PCB2 | PCB1 | PCB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PCR[7:0] : Precharge current R.

PCG[7:0] : Precharge current G.

PCB[7:0] : Precharge current B.

* Precharge current = setting value * 8uA.

DRIVING_CURRENT_R (10h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | DCR7 | DCR6 | DCR5 | DCR4 | DCR3 | DCR2 | DCR1 | DCR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DRIVING_CURRENT_G (11h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | DCG7 | DCG6 | DCG5 | DCG4 | DCG3 | DCG2 | DCG1 | DCG0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DRIVING_CURRENT_B (12h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | DCB7 | DCB6 | DCB5 | DCB4 | DCB3 | DCB2 | DCB1 | DCB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DCR[7:0] : DCR driving current R.

DCG[7:0] : DCG driving current G.

DCB[7:0] : DCB driving current B.

* Driving current = setting value * 1uA.

DISPLAY_MODE_SET(13h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | SWAP | SM | RD | CD | - | SPT | DC1 | DC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SWAP : RGB swap.

| | SWAP = 0 | | | SWAP = 1 | | |
|--------|----------|---|---|----------|---|---|
| Input | R | G | B | R | G | B |
| Output | R | G | B | B | G | R |

SM : Scan mode.

RD : Row scan shift direction.

| SM | RD | G[127:0] | | | | | | | | | |
|----|----|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | 2 | ... | | | | 125 | 126 | 127 |
| 0 | 1 | 127 | 126 | 125 | ... | | | | 2 | 1 | 0 |
| 1 | 0 | 0 | 2 | 4 | ... | 126 | 1 | 3 | ... | 125 | 127 |
| 1 | 1 | 127 | 125 | 123 | ... | 1 | 126 | 124 | ... | 2 | 0 |

CD : Column data shift direction.

When CD= 0, D0 to D159 shift

When CD= 1, D159 to D0 shift

SPT : Split

When SPT = 0, One screen mode

When SPT = 1, Two screen mode

DC[1:0] : Column data display control.

| DC1 | DC0 | Data Output |
|-----|-----|-------------------------|
| 0 | 0 | Normal Display(default) |
| 0 | 1 | All Low Display |
| 1 | 0 | All High Display |
| 1 | 1 | Reserved |

RGB_IF (14h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | RIM1 | RIM0 | - | - | - | EIM |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

RIM[1:0] : RGB interface mode.

| RIM1 | RIM0 | Result |
|------|------|----------------------|
| 0 | 0 | 18_Bit RGB interface |
| 0 | 1 | 16_Bit RGB interface |
| 1 | 0 | 6_Bit RGB interface |
| 1 | 1 | Reserved |

EIM : External interface mode.

When EIM = 0, RGB

When EIM = 1, MPU

RGB_POL (15h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|--------|------|------|------|
| R/W | RES | RES | ENP | DOP | VSYOEN | RES | RES | RES |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VSYOEN : Vsync. Output enable(0 : VSYNCO disable).

DOP : Dot clock polarity(0 : sampled at rising edge).

ENP : Enable polarity(0 : active low).

Note) All reserved signals(RES) must write to '0'.

MEMORY_WRITE_MODE (16h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | DFM1 | DFM0 | TRI | - | HC | VC | HV |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

DFM[1:0], TRI :

| DFM1 | DFM0 | TRI | BIT | Result |
|------|------|-----|--------|-------------------------------|
| 0 | 0 | X | 18_bit | Single transfer, 262k support |
| 0 | 1 | X | 16_bit | Single transfer, 65k support |
| 1 | 0 | X | 9_bit | Dual transfer, 262k support |
| 1 | 1 | 0 | 8_bit | Dual transfer, 65k support |
| 1 | 1 | 1 | 8_bit | Triple transfer, 262k support |

HC : Horizontal address increment/decrement.

When HC= 0, Horizontal address counter is decreased

When HC= 1, Horizontal address counter is increased

VC : Vertical address increment/decrement.

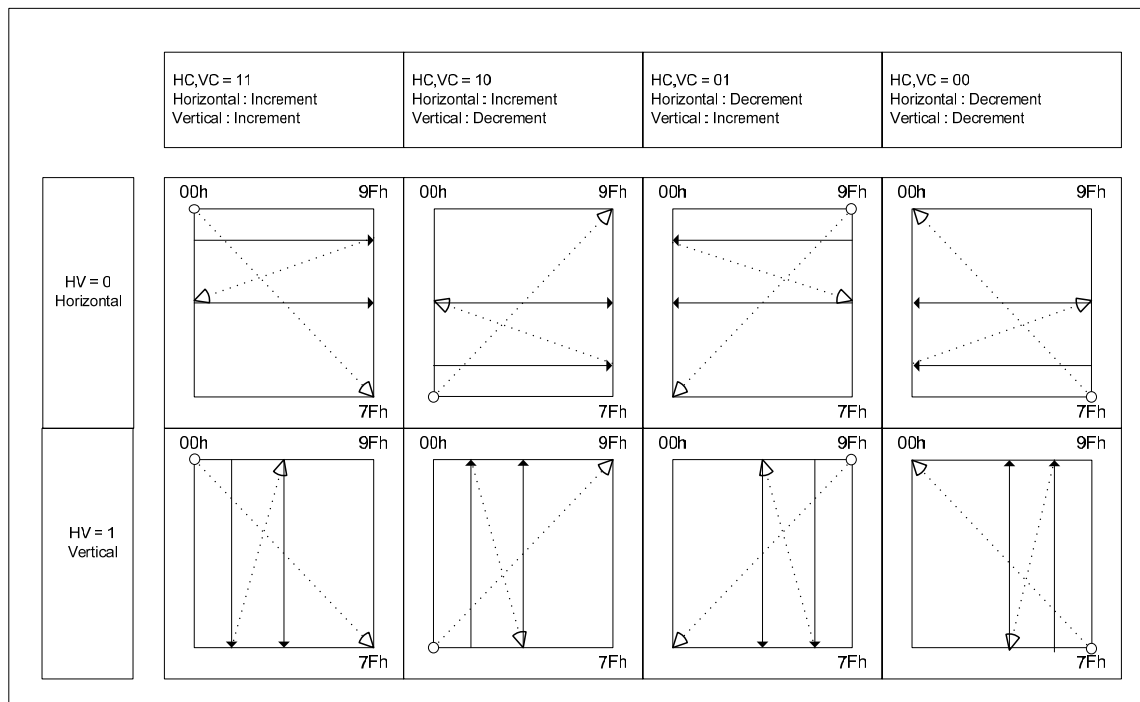
When VC= 0, Vertical address counter is decreased

When VC= 1, Vertical address counter is increased

HV : Set the automatic update method of the AC after the data is written to the DDRAM.

When HV= 0, The data is continuously written horizontally

When HV= 1, The data is continuously written vertically



MX1_ADDR (17h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | MX1_7 | MX1_6 | MX1_5 | MX1_4 | MX1_3 | MX1_2 | MX1_1 | MX1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MX2_ADDR (18h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | MX2_7 | MX2_6 | MX2_5 | MX2_4 | MX2_3 | MX2_1 | MX2_1 | MX2_0 |
| Default | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

MY1_ADDR (19h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | MY1_7 | MY1_6 | MY1_5 | MY1_4 | MY1_3 | MY1_2 | MY1_1 | MY1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MY2_ADDR (1Ah)

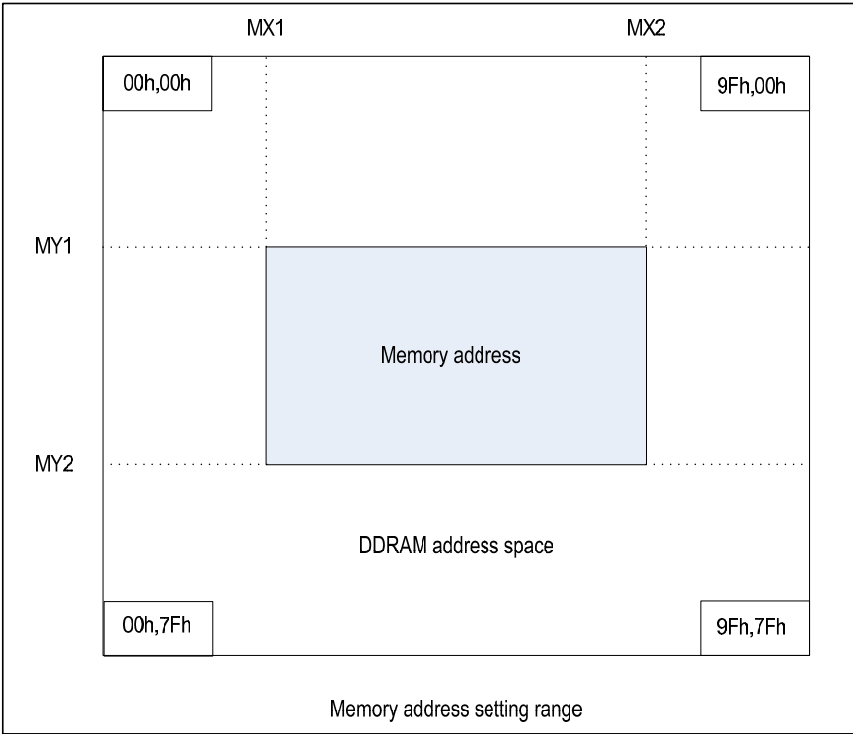
| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | MY2_7 | MY2_6 | MY2_5 | MY2_4 | MY2_3 | MY2_1 | MY2_1 | MY2_0 |
| Default | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

MX1[7:0] / MX2[7:0]

Specify the horizontal start/end position of a window for access in memory. Data can be written to DDRAM from the address specified by MX1[7:0] to the address specified by MX2[7:0].

MY1[7:0] / MY2[7:0]

Specify the vertical start/end position of a window for access in memory. Data can be written to DDRAM from the address specified by MY1[7:0] to the address specified by MY2[7:0].



MEMORY_ACCESSPOINTER X (20h)

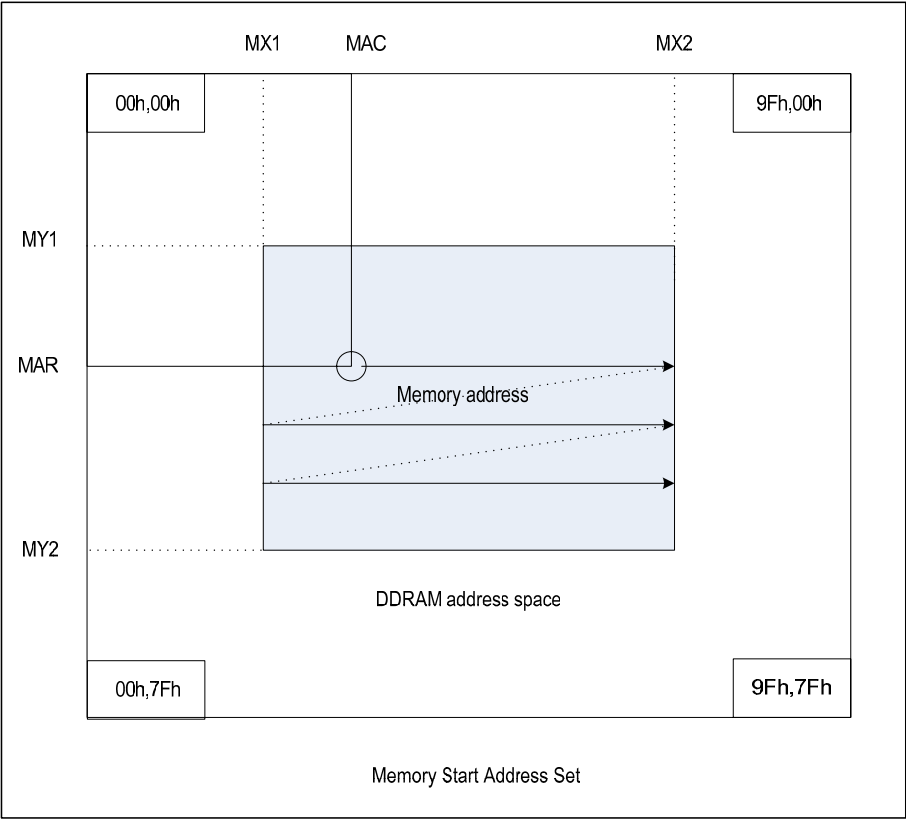
| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | MAC7 | MAC6 | MAC5 | MAC4 | MAC3 | MAC2 | MAC1 | MAC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MEMORY_ACCESSPOINTER Y (21h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | MAR7 | MAR6 | MAR5 | MAR4 | MAR3 | MAR2 | MAR1 | MAR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MAC[7:0] / MAR[7:0]

Specify the horizontal start/vertical start position of a window for write in memory
Data can be written to DDRAM from MAC[7:0]/MAR7:0] to MX2[7:0]/MY2[7:0]



DDRAM_DATA_ACCESS_PORT (22h)

| | Bit 17 | Bit16 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| R/W | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Default | R | | | | | | G | | | | | | B | | | | | |

DDRAM[17:0] : After index register 22h is select, Internal DDRAM memory can be accessed.

GRAY_SCALE_TABLE_INDEX (50h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| R/W | IGAMMA7 | IGAMMA6 | IGAMMA5 | IGAMMA4 | IGAMMA3 | IGAMMA2 | IGAMMA1 | IGAMMA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IGAMMA[7:0] : Index register for gamma table.

There are 32 entry of odd IGAMMA.

GRAY_SCALE_TABLE_DATA (51h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| R/W | DGAMMA7 | DGAMMA6 | DGAMMA5 | DGAMMA4 | DGAMMA3 | DGAMMA2 | DGAMMA1 | DGAMMA0 |

DGAMMA[7:0] : Data register for gamma table.

If DGAMMA is even, $DGAMMA\ n = (DGAMMA\ n-1 + DGAMMA\ n+1)/2$

DGAMMA RED (Index Register 00H ~ 1FH)

| Index Register | IGAMMA | Reset Value |
|----------------|--------|-------------|
| 00h | 1 | 1 |
| 01h | 3 | 5 |
| 02h | 5 | 9 |
| ⋮ | ⋮ | ⋮ |
| 1Eh | 61 | 121 |
| 1Fh | 63 | 125 |

DGAMMA GREEN (Index Register 20H ~ 3FH)

| Index Register | IGAMMA | Reset Value |
|----------------|--------|-------------|
| 20h | 1 | 1 |
| 21h | 3 | 5 |
| 22h | 5 | 9 |
| ⋮ | ⋮ | ⋮ |
| 3Eh | 61 | 121 |
| 3Fh | 63 | 125 |

DGAMMA BLUE (Index Register 40H ~ 5FH)

| Index Register | IGAMMA | Reset Value |
|----------------|--------|-------------|
| 40h | 1 | 1 |
| 41h | 3 | 5 |
| 42h | 5 | 9 |
| ⋮ | ⋮ | ⋮ |
| 5Eh | 61 | 121 |
| 5Fh | 63 | 125 |

DUTY (28h)

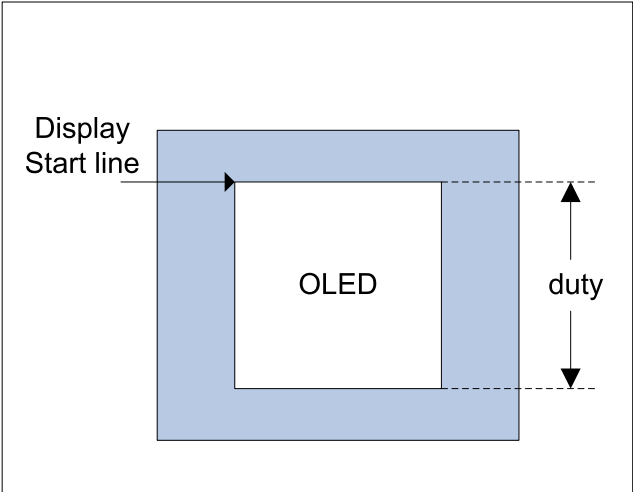
| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | DUTY7 | DUTY6 | DUTY5 | DUTY4 | DUTY3 | DUTY2 | DUTY1 | DUTY0 |
| Default | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

DUTY[7:0] : Display duty ratio(16~127).

DSL (29h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | DSL7 | DSL6 | DSL5 | DSL4 | DSL3 | DSL2 | DSL1 | DSL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DSL[7:0] : Display start line(0~127-16).



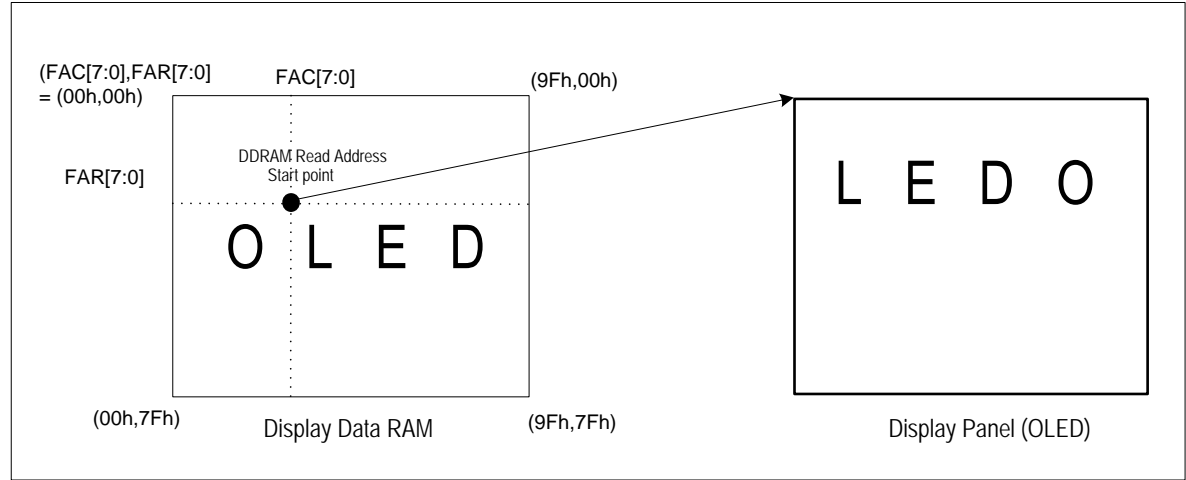
D1_DDRAM_FAC (2Eh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | FAC7 | FAC6 | FAC5 | FAC4 | FAC3 | FAC2 | FAC1 | FAC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D1_DDRAM_FAR (2Fh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | FAR7 | FAR6 | FAR5 | FAR4 | FAR3 | FAR2 | FAR1 | FAR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FAC[7:0] : First screen display horizontal address for display.
FAR[7:0] : First screen display vertical address for display.



D2_DDRAM_SAC (31h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | SAC7 | SAC6 | SAC5 | SAC4 | SAC3 | SAC2 | SAC1 | SAC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D2_DDRAM_SAR (32h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | SAR7 | SAR6 | SAR5 | SAR4 | SAR3 | SAR2 | SAR1 | SAR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SAC[7:0] : Second screen display horizontal address for display.
SAR[7:0] : Second screen display vertical address for display.

SCR1_FX1 (33h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FX1_7 | FX1_6 | FX1_5 | FX1_4 | FX1_3 | FX1_2 | FX1_1 | FX1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SCR1_FX2 (34h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FX2_7 | FX2_6 | FX2_5 | FX2_4 | FX2_3 | FX2_2 | FX2_1 | FX2_0 |
| Default | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

SCR1_FY1 (35h)

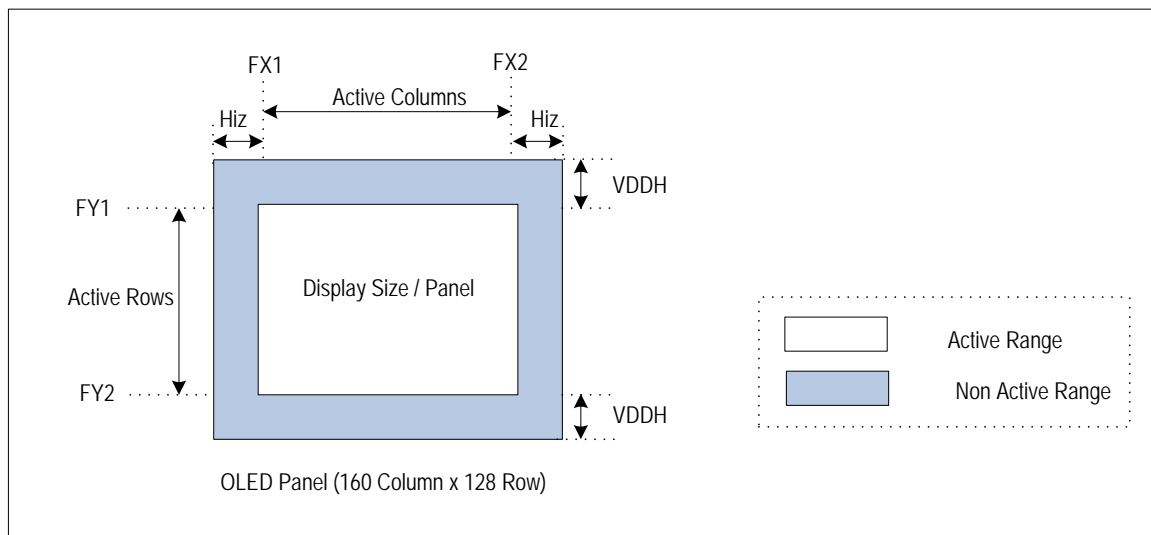
| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FY1_7 | FY1_6 | FY1_5 | FY1_4 | FY1_3 | FY1_2 | FY1_1 | FY1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SCR1_FY2 (36h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FY2_7 | FY2_6 | FY2_5 | FY2_4 | FY2_3 | FY2_2 | FY2_1 | FY2_0 |
| Default | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FX1[7:0] / FX2[7:0] : The start/end address of active column outputs for the first screen (00h ~ 9Fh).
(FX1[7:0] < FX2[7:0])

FY1[7:0] / FY2[7:0] : The start/end address of active row outputs for the second screen (00h ~ 7Fh).
(FY1[7:0] < FY2[7:0])



The row outputs out of active area are always VDDH excluding display off.

SCR2_SX1 (37h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SX1_7 | SX1_6 | SX1_5 | SX1_4 | SX1_3 | SX1_2 | SX1_1 | SX1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SCR2_SX2 (38h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SX2_7 | SX2_6 | SX2_5 | SX2_4 | SX2_3 | SX2_2 | SX2_1 | SX2_0 |
| Default | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

SCR2_SY1 (39h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SY1_7 | SY1_6 | SY1_5 | SY1_4 | SY1_3 | SY1_2 | SY1_1 | SY1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SCR2_SY2 (3Ah)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SY2_7 | SY2_6 | SY2_5 | SY2_4 | SY2_3 | SY2_2 | SY2_1 | SY2_0 |
| Default | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SX1[7:0] : 2nd Screen display size horizontal start.

SX2[7:0] : 2nd Screen display size horizontal end.

SY1[7:0] : 2nd Screen display size vertical start.

SY2[7:0] : 2nd Screen display size vertical end.

SCREEN_SAVER_CONTEROL (3Bh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | SSA1 | SSA0 | - | SSC1 | SSC0 | - | SSM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SSA[1:0] : 1st, 2nd Screen auto sleep saver.

| SSA1 | SSA0 | 2 nd Screen | 1 st Screen |
|------|------|------------------------|------------------------|
| 0 | 0 | OFF | OFF |
| 0 | 1 | OFF | ON |
| 1 | 0 | ON | OFF |
| 1 | 1 | ON | ON |

SSC[1:0] : 1st, 2nd Screen on/off saver control.

| SSC1 | SSC0 | 2 nd Screen | 1 st Screen |
|------|------|------------------------|------------------------|
| 0 | 0 | OFF | OFF |
| 0 | 1 | OFF | ON |
| 1 | 0 | ON | OFF |
| 1 | 1 | ON | ON |

SSM : Screen Saver Mode on/off(0: off, 1: on).

When SSM= 0, Screen Saver mode OFF(default)

When SSM= 1, Screen saver mode ON

SS_SLEEP_TIMER (3Ch)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | SST7 | SST6 | SST5 | SST4 | SST3 | SST2 | SST1 | SST0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SST [7:0] : Screen saver sleep timer.

Note) Based on 64 frames sync.

Ex) when setting value = 10 :

Screen saver will enter sleep mode after 10*64 frame display.

SCREEN_SAVER_MODE (3Dh)

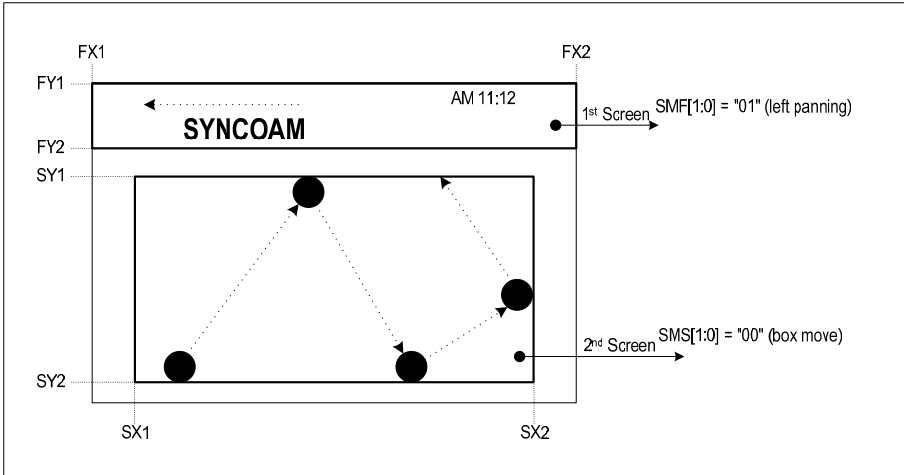
| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|------|------|------|------|------|------|
| R/W | - | - | SMS1 | SMS0 | - | - | SMF1 | SMF0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SMF[1:0] : 1st Screen mode set.

| SMF1 | SMF0 | 1 st Screen |
|------|------|------------------------|
| 0 | 0 | Reserved |
| 0 | 1 | Left Panning |
| 1 | 0 | Right Panning |
| 1 | 1 | Reserved |

SMS[1:0] : 2nd Screen mode set.

| SMS1 | SMS0 | 2 nd Screen |
|------|------|------------------------|
| 0 | 0 | Box move |
| 0 | 1 | Log on |
| 1 | 0 | Reserved |
| 1 | 1 | Wrap_around |



SS_SCR1_FU (3Eh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FSUT7 | FSUT6 | FSUT5 | FSUT4 | FSUT3 | FSUT2 | FSUT1 | FSUT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FSUT[7:0] : 1st Screen update timer based on frame sync.

SS_SCR1_MXY (3Fh)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | FSMS7 | FSMS6 | FSMS5 | FSMS4 | FSMS3 | FSMS2 | FSMS1 | FSMS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FSMS[7:0] : 1st Screen moving step.

FSMS[7:4] : Vertical moving step.

FSMS[3:0] : Horizontal moving step.

SS_SCR2_FU (40h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SSUT7 | SSUT6 | SSUT5 | SSUT4 | SSUT3 | SSUT2 | SSUT1 | SSUT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SSUT[7:0] : 2nd Screen update timer based on frame sync.

SS_SCR2_MXY (41h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | SSMS7 | SSMS6 | SSMS5 | SSMS4 | SSMS3 | SSMS2 | SSMS1 | SSMS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SSMS[7:0] : 2nd Screen moving step.

SSMS[7:4] : Vertical moving step.

SSMS[3:0] : Horizontal moving step.

MOVING_DIRECTION (42h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------|------|-------|-------|------|------|-------|-------|
| R/W | - | - | SSMD1 | SSMD0 | - | - | FSMD1 | FSMD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FSMD[1:0] : 1st Screen moving direction.

| FSMD1 | FSMD0 | 1 st Screen |
|-------|-------|------------------------|
| 0 | 0 | UP, LEFT |
| 0 | 1 | UP, RIGHT |
| 1 | 0 | DOWN, LEFT |
| 1 | 1 | DOWN, RIGHT |

SSMD[1:0] : 2nd Screen moving direction.

| SSMD1 | SSMD0 | 2 nd Screen |
|-------|-------|------------------------|
| 0 | 0 | UP, LEFT |
| 0 | 1 | UP, RIGHT |
| 1 | 0 | DOWN, LEFT |
| 1 | 1 | DOWN, RIGHT |

SS_SCR2_SX1 (47h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W | ISX1_7 | ISX1_6 | ISX1_5 | ISX1_4 | ISX1_3 | ISX1_2 | ISX1_1 | ISX1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SS_SCR2_SX2 (48h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W | ISX2_7 | ISX2_6 | ISX2_5 | ISX2_4 | ISX2_3 | ISX2_2 | ISX2_1 | ISX2_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SS_SCR2_SY1 (49h)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W | ISY1_7 | ISY1_6 | ISY1_5 | ISY1_4 | ISY1_3 | ISY1_2 | ISY1_1 | ISY1_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SS_SCR2_SY2 (4Ah)

| | Bit 7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W | ISY2_7 | ISY2_6 | ISY2_5 | ISY2_4 | ISY2_3 | ISY2_2 | ISY2_1 | ISY2_0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ISX1[7:0] : 2nd Screen image box horizontal start address.

ISX2[7:0] : 2nd Screen image box horizontal end address.

ISY1[7:0] : 2nd Screen image box vertical start address.

ISY2[7:0] : 2nd Screen image box vertical end address.

6. Electric Characteristics

1) Absolute Maximum Rating

| ITEM | SYMBOL | CONDITION | PORT | RATINGS | UNIT |
|---------------------|--------|---|-------|------------------|------|
| Supply voltage | VDD | VSS/VSSH/ VDSH(0V) Reference Ta = +25℃ | VDD | - 0.3 ~ +4.0 | V |
| | VDDH | | VDDH | - 0.3 ~ +19.5 | V |
| | VDDIO | | VDDIO | - 0.3 ~ +4.0 | V |
| Input voltage | VI | | *1 | - 0.3 ~ +VDD+0.3 | V |
| Storage temperature | Tstg | | | - 65 ~ +150 | ℃ |

*1 : DB[17:0], CPU, PS, CSB, RS, RDB, WRB, RESETB.

2) Recommended Operation Conditions

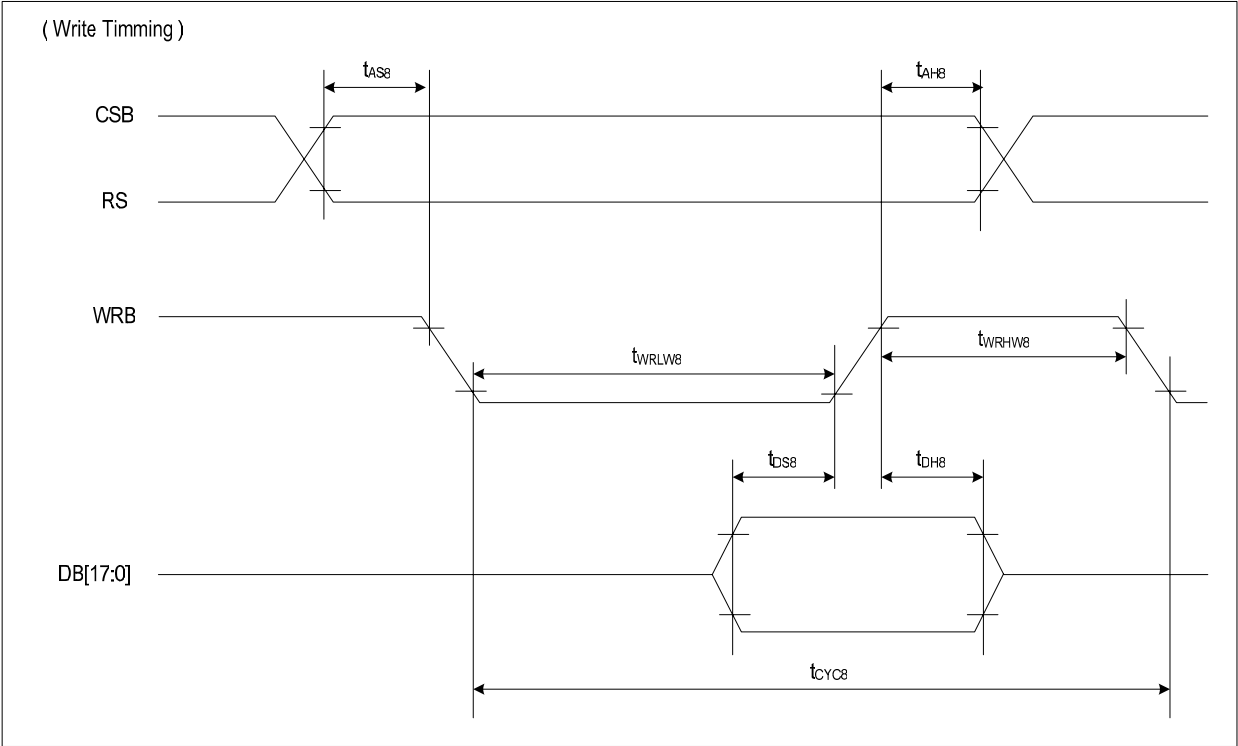
| ITEM | SYMBOL | PORT | MIN | TYP | MAX | UNIT | REMARK |
|-----------------------|--------|----------|------|-----|------|------|--------|
| Supply voltage | VDD | VDD | 2.4 | 2.8 | 3.3 | V | |
| | VDDH | VDDH | 8.0 | 16 | 18.0 | V | |
| | VDDIO | VDDIO | 1.6 | - | 3.3 | V | |
| Operating voltage | VDC | S[479:0] | 0 | 16 | 18.0 | V | |
| Operation temperature | Topr | | - 40 | | 85 | ℃ | |

3) DC Characteristics

| ITEM | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT | PORT |
|--|--------|--|---------|-----|-----|------|------|
| High level input voltage | VIH | | 0.8XVDD | | VDD | V | |
| Low level input voltage | VIL | | 0 | | 0.4 | V | |
| High level output voltage | VOH1 | IOH = -0.4mA | VDD-0.4 | | | V | |
| Low level output voltage | VOL1 | IOL = -0.4mA | | | 0.4 | V | |
| High level output voltage | VOH2 | IOH = -0.1mA | VDD-0.4 | | | V | |
| Low level output voltage | VOL2 | IOL = -0.1mA | | | 0.4 | V | |
| Input leakage current | ILI | VI = VSS or VDD | -1 | | 1 | uA | |
| Output leakage current | ILO | VI = VSS or VDD | -1 | | 1 | uA | |
| Static current (1) | ISB | CSB = VDD, VDD = 2.8V Ta = 25℃ | | | TBD | uA | |
| Static current (2) | SITBP | CSB = VDD, VDD = 2.8V Ta = 25℃, Power save mode | | | TBD | uA | |
| Current Consumption (1) | IVDD1 | VDD = 2.8V IDC = 200uA | | | TBD | uA | |
| Current Consumption (2) | IVDD2 | VDD = 2.8V IDC = 100uA | | | TBD | uA | |
| Current Consumption (3) | IVDD3 | VDD = 2.8V IDC = 50uA | | | TBD | uA | |
| Oscillator frequency | FOSC1 | VDD = 2.8V Ta = 25℃ | TBD | | TBD | MHz | |
| Oscillator frequency By external resistor | FSO1 | RF = TBDkΩ | TBD | | TBD | MHz | |
| Frame scan rate | Frame | VDD = 2.8V, Ta = 25℃ | 75 | 90 | 150 | Hz | |
| Column output current range | IDC | 4 < VDC < VDDH -2V | 0 | | 255 | uA | |
| Column output current match | IDCM | 4 < VDC < VDDH -2V | | | ±3 | % | |
| Row switch on current sink | IDR | Common is on, IDR=TBDuA, PWM TBDcks | | | 120 | mA | |
| Row switch on resistance | RDR | Common is on, VDC IFM = 30 mA | | 20 | 25 | Ω | |

4) AC Characteristics

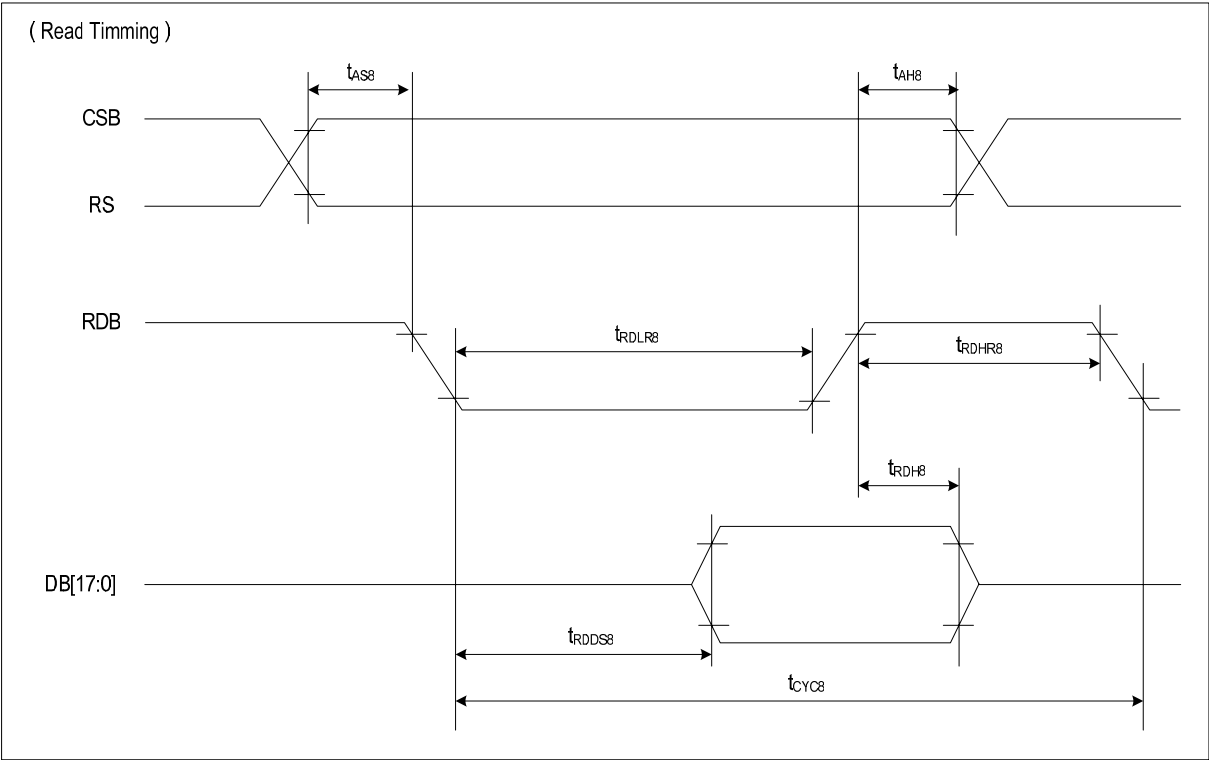
4-1) System BUS Read/Write Timing (80 series CPU interface)



(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|-----------------------|-------------|-----------|-----|-----|------|----------|
| Address hold timing | t_{AH8} | - | 5 | - | ns | CSB |
| Address setup timing | t_{AS8} | - | 5 | - | ns | RS |
| System cycle timing | t_{CYC8} | - | 100 | - | ns | WRB |
| Write "L" pulse width | t_{WRLW8} | - | 45 | - | ns | |
| Write "H" pulse width | t_{WRHW8} | - | 45 | - | ns | |
| Data setup timing | t_{DS8} | - | 30 | - | ns | DB[17:0] |
| Data hold timing | t_{DH8} | - | 10 | - | ns | |

notice) All the timing reference is 10% and 90% of VDD.

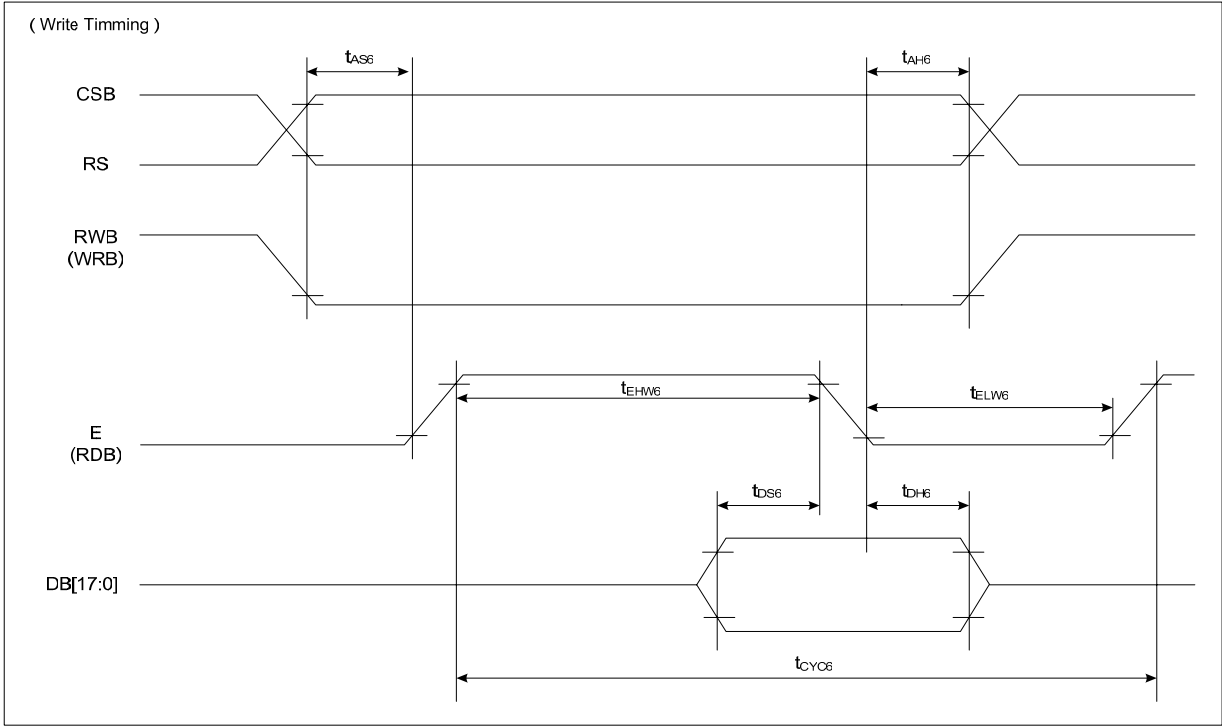


(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|-----------------------------|-------------|------------|-----|-----|------|----------|
| Address hold timing | t_{AH8} | - | 5 | - | ns | CSB |
| Address setup timing | t_{AS8} | - | 5 | - | ns | RS |
| System cycle timing | t_{CYC8} | - | 200 | - | ns | RDB |
| Read "L" pulse width | t_{RDLR8} | - | 90 | - | ns | RDB |
| Read "H" pulse width | t_{RDHR8} | - | 90 | - | ns | RDB |
| Read data output delay time | t_{RDD8} | CL = 15 pF | - | 60 | ns | DB[17:0] |
| Data hold timing | t_{RDH8} | CL = 15 pF | 0 | - | ns | DB[17:0] |

notice) All the timing reference is 10% and 90% of VDD.

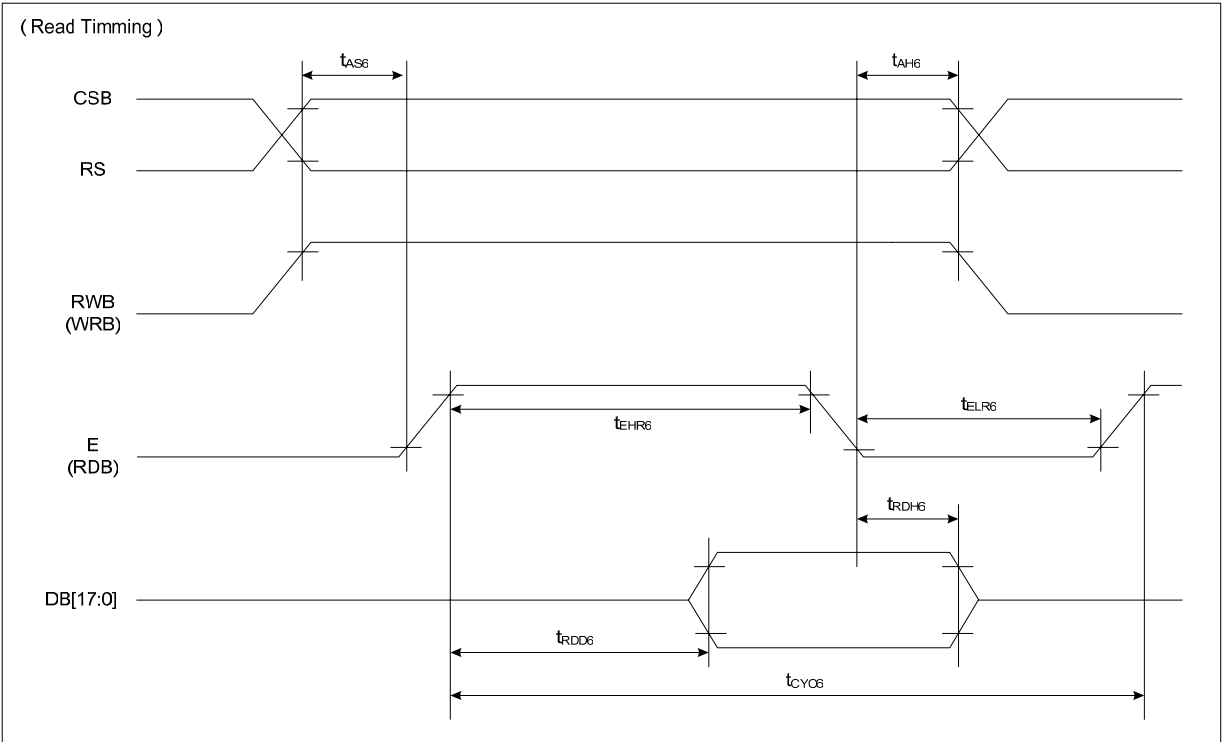
4-2) System BUS Read/Write Timing (68 series CPU interface)



(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|-----------------------|--------|-----------|-----|-----|------|----------|
| Address hold timing | tAH6 | - | 5 | - | ns | CSB |
| Address setup timing | tAS6 | - | 5 | - | ns | RS |
| System cycle timing | tCYC6 | - | 100 | - | ns | E |
| Write "L" pulse width | tELW6 | - | 45 | - | ns | E |
| Write "H" pulse width | tEHW6 | - | 45 | - | ns | E |
| Data setup timing | tDS6 | - | 40 | - | ns | DB[17:0] |
| Data hold timing | tDH6 | - | 10 | - | ns | DB[17:0] |

notice) All the timing reference is 10% and 90% of VDD.

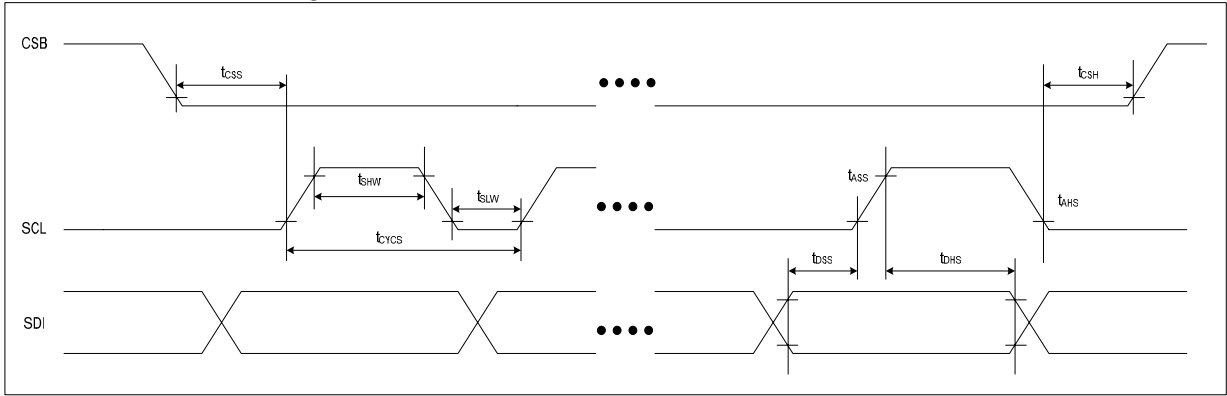


(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|-----------------------------|--------|------------|-----|-----|------|----------|
| Address hold timing | tAH6 | - | 10 | - | ns | CSB |
| Address setup timing | tAS6 | - | 10 | - | ns | RS |
| System cycle timing | tCYC6 | - | 200 | - | ns | E |
| Read "L" pulse width | tELR6 | - | 90 | - | ns | E |
| Read "H" pulse width | tEHR6 | - | 90 | - | ns | E |
| Read data output delay time | tRDD6 | CL = 15 pF | 0 | 70 | ns | DB[17:0] |
| Data hold timing | tRDH6 | CL = 15 pF | - | - | ns | DB[17:0] |

notice) All the timing reference is 10% and 90% of VDD.

4-3) Serial Interface Timing

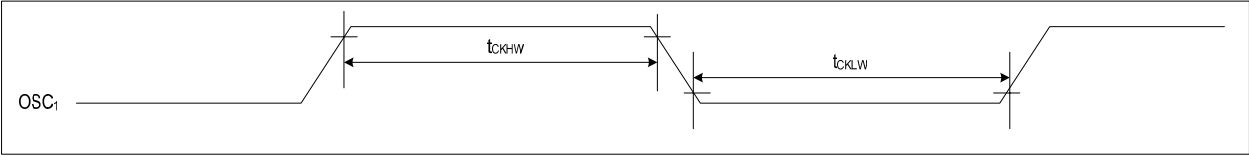


(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|---------------------|--------|-----------|-----|-----|------|------|
| Serial clock cycle | tcycs | - | 60 | - | ns | SCL |
| SCL "H" pulse width | tshw | - | 25 | - | ns | SCL |
| SCL "L" pulse width | tslw | - | 25 | - | ns | SCL |
| Data setup timing | tdss | - | 25 | - | ns | SDI |
| Data hold timing | tdhs | - | 25 | - | ns | SDI |
| CSB-SCL timing | tcss | - | 25 | - | ns | CSB |
| CSB-hold timing | tchsh | - | 25 | - | ns | CSB |

notice) All the timing reference is 10% and 90% of VDD.

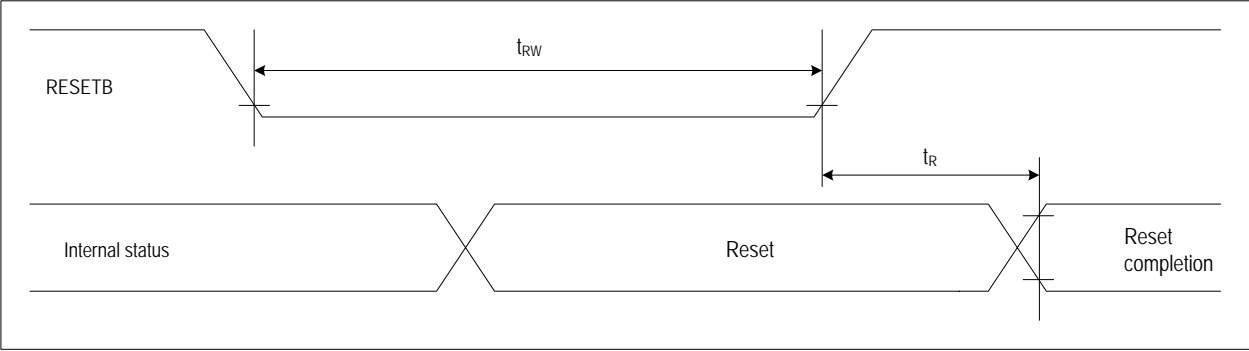
4-4) External Clock Input Timing



(VDD = 2.8V, Ta = 25℃)

| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|--------------------------|--------|-----------|-----|-----|------|------|
| Osc1 "H" pulse width (1) | tCKHW1 | | TBD | TBD | us | OSC1 |
| Osc1 "L" pulse width (1) | tCKLW1 | | TBD | TBD | us | |
| Osc1 "H" pulse width (2) | tCKHW2 | | TBD | TBD | us | OSC1 |
| Osc1 "L" pulse width (2) | tCKLW2 | | TBD | TBD | us | |

4-5) Reset Input Timing



(VDD = 2.8V, Ta = 25℃)

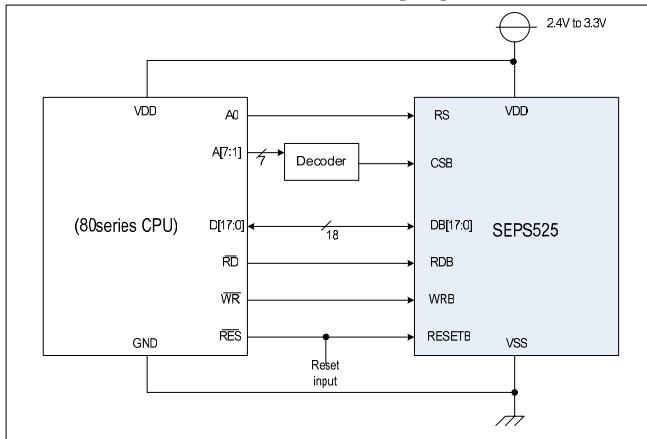
| ITEM | SYMBOL | CONDITION | MIN | MAX | UNIT | PORT |
|------------------------|--------|-----------|-----|-----|------|--------|
| Reset time | tR | | | 1.5 | us | |
| RESETB "L" pulse width | tRW | | 5 | | us | RESETB |

7. Application Example

1) Connection With CPU

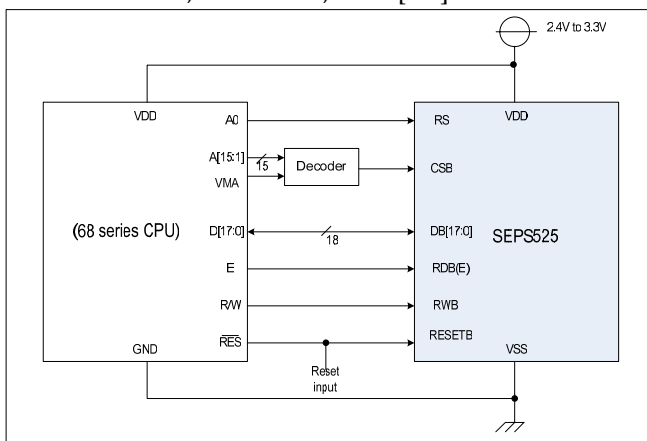
1-1) 80 Series CPU Interface(18-bit bus)

=> PS = "1", CPU = "0", DFM[1:0] = "00"

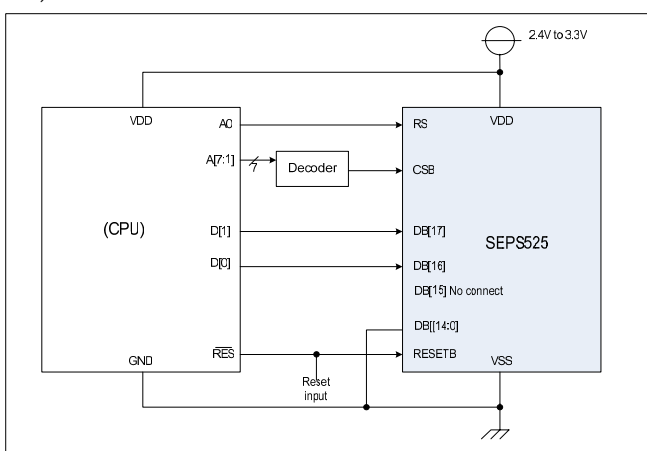


1-2) 68 Series CPU Interface(18-bit bus)

=> PS = "1", CPU = "1", DFM[1:0] = "00"



1-3) CPU Connection With Serial Interface



Revision History

| Rev. # | Contents | page | Name | Date |
|--------|--------------------------|--------|---------------|--------------|
| 0.0 | Draft | | YK Kim/ A Ahn | 2005. 12. 07 |
| 0.20 | Address 04h, 15h Changed | P20,24 | YK Kim/ A Ahn | 2006. 04. 14 |